FireFly™ Optical

ETUO 25G x4 Datasheet

Revision 0.2, June 2019

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Patents

Multiple patents are issued and pending.

Table of Contents

Change History

Revision #	Reason	Date
Revision 0.1	Draft	04/25/2019
Revision 0.2	Edits	06/19/2019

1 Introduction

1.1 *Product Features*

The FireFly Micro Flyover System is the first inside the box interconnect system that gives the designer a choice of using either high performance optical or low-cost copper interconnects interchangeably. The FireFly system enables chip-to-chip, board-to-board and system-to-system connectivity at baud rates up to 50 Gbps. The FireFly product line offers passive copper cables, passive and active equalised copper cables as well as optical assemblies with different widths and data rates.

By taking the data connections “off-board” with FireFly flyover cables, the signal integrity design of a host board is made significantly easier, and the electrical performance improved allowing for lower power consumption and cheaper board materials. By allowing data to fly over these lossy materials and signal degrading features negates the need for the layout complexities and signal drive conditions that are required to design for high speed signalling.

Unlike existing optical engine-based solutions, thermal operating conditions are acknowledged and designed for by including an integral heat sink. The heat sink is available in several default designs to allow for air cooling or cold plate liquid cooling. In addition, the flexible design accepts customer specific heat sinks for easy integration into existing thermal solutions.

Due to Samtec’s extensive catalogue of connector solutions, the copper FireFly assembly is made even more powerful by allowing use of different connector types for the far end. This enables the seamless connection between new boards and existing products without forcing a redesign.

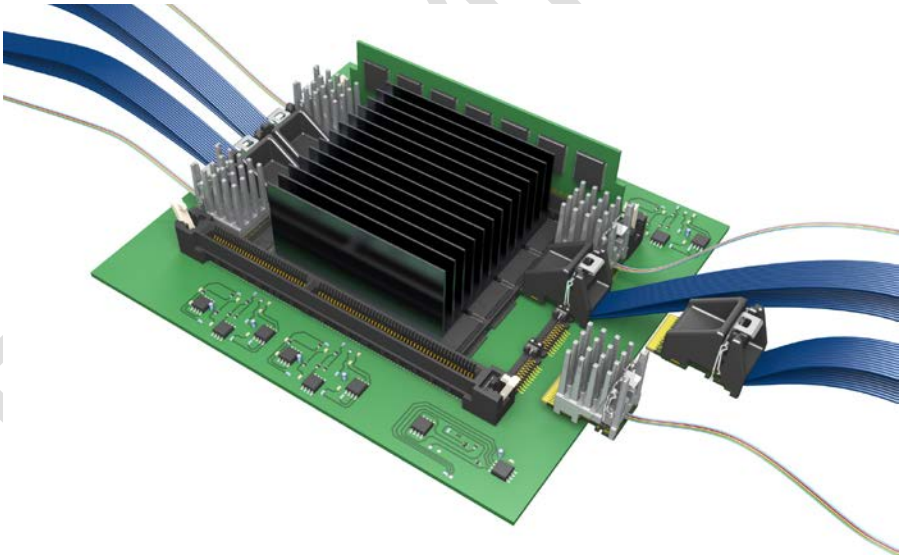


Figure 1: FireFly Application using Copper and Optical Assemblies

1.2 System Components

1.2.1 On Board Connector and Transceiver

The FireFly Connector system is a two-part connector designed for applications up to 50 Gbps. It is based on two connectors, a micro high-speed edge connector (UEC5, shown rear left) with two rows of 19 positions providing 12 differential lanes and a 10-position positive latch connector (UCC8, shown front right).

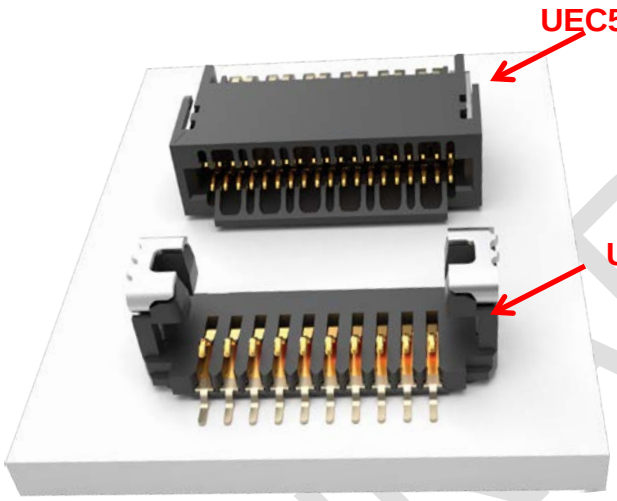


Figure 2: FireFly Connector System

The UEC5 connector is used to connect the high-speed data signals from the host system to the inputs of the optical or copper FireFly assemblies.

The UCC8 connector provides mechanical support in conjunction with a mechanical latch on the FireFly assembly. In addition, it provides power and low speed communications for optical assemblies.

1.2.2 Copper Cables

FireFly copper cables fully compatible with the ETUO-B04 are available based on Samtec's 100Ω 34 AWG FireFly copper cables are available based on Samtec's 50Ω 38 AWG, Micro coax ribbon cable. This cable provides performance up to 28 Gbps on eight or twelve 100Ω differential lanes and comes as standard with a second FireFly connector on end two.

Figure 3 represents a FireFly flyover copper cable with four channel duplex and low-profile housing. It shows the detail of the ECUE FireFly copper cable.

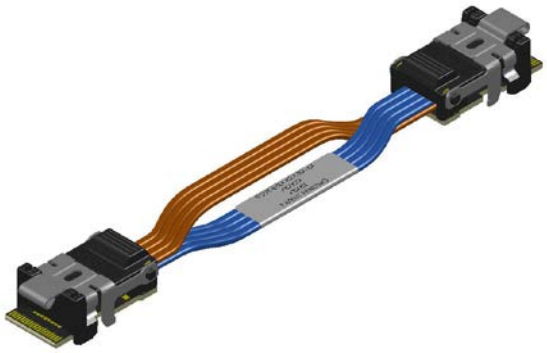


Figure 3: ECUE x4 (8 pairs) With Low Profile Housing

- Data “flies” over the PCB for simplified routing and enhanced signal integrity
- Future-proof design allows for an easy upgrade from electrical to optical using the same connector set
- Compatible with Samtec’s UCC8 / UEC5 Series connector set
- Evaluation kits available
- Rugged positive latching mechanism

Samtec’s design flexibility also allows for the ECUE Cable to use nearly any connector in our Full Line Catalog for the second end. Samtec can also adjust how the signals are routed within the cables, as well as assist with high speed analysis by reviewing your system and providing recommendations for appropriate cable solutions based on signal requirements.

- Edge Card
- SEARAY™
- Q Rate®
- Q Series®
- Edge Rate™

Figure 4: ECUE End 2 Options

For easy interchangeability with FireFly optical assemblies, the copper cable can be ordered with on board 100 nF decoupling capacitors and can be configured with an identical pin out to the optical assembly.

Please contact HDR@samtec.com for further information.

1.3 *Evaluation Board*

The FireFly evaluation kit consist of a break-out board connecting a FireFly socket (UEC5 and UCC8 connectors) to a 2x12 Bull's Eye connector landing pads and bringing low speed signals and power rails to various standard connectors.

A mating Samtec Bull's Eye connector with 24 cables terminated with SMA connectors allows for connecting all 12 channels to test equipment. A second Bull's Eye connector landing pad provides standard open and thru circuits to enable de-embedding of the Bull's Eye and PCB effects on the high-speed signals.

Kit includes the following items:

- 1 FireFly PCB break-out board
- 1 Bull's Eye cable assembly
- 1 Bull's Eye cable removal tool
- 1 Raspberry Pi3
- 1 Ribbon Cable (20 x 2)

Figure 5: FireFly Evaluation Kit

The part number to purchase the 25 Gbps evaluation kit is FIK-FIREFLY-06.

Samtec has a GUI that allows easy control of user configurable parameters. A representation of the GUI is shown in Figure 6. This user interface is available by contacting FireFly@samtec.com.

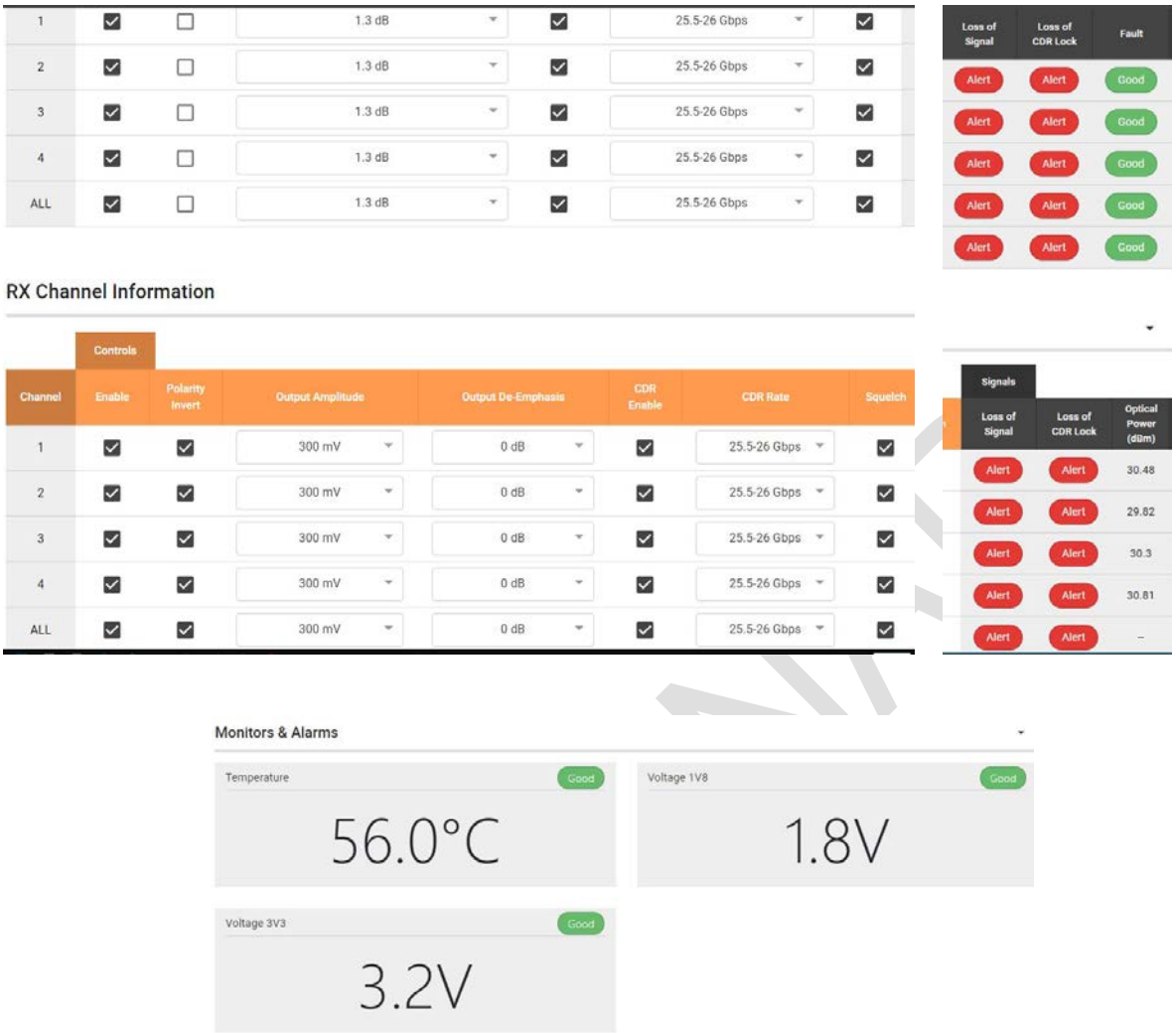


Figure 6: GUI Controls, Signals, Voltage and Temperature Monitor

1.4 *Temperature Performance*

Samtec recognises that different applications have different thermal requirements. The temperature ranges for the different FireFly components are shown in Table 1.

Series		Temperature Range	
UEC5	FireFly data connector	-55 °C to 125 °C	“Military”
UCC8	FireFly low speed connector	-55 °C to 125 °C	“Military”
ECUE	FireFly copper assembly	-25 °C to 105 °C	
ECUO	14G/28G optical assembly	0 °C to 70 °C	“Commercial”
ETUO	Extended Temperature 10G/25G optical assemblies	-40 °C to +85 °C	“Extended Industrial”
PCUO	PCIe over FireFly connector	0 °C to 70 °C	“Commercial”
PTUO	PCIe over FireFly extended temperature	-40 °C to +85 °C	“Extended Industrial”

Table 1: Temperature Ranges for FireFly Components

1.5 *Dimensions*

1.5.1 Copper Cable

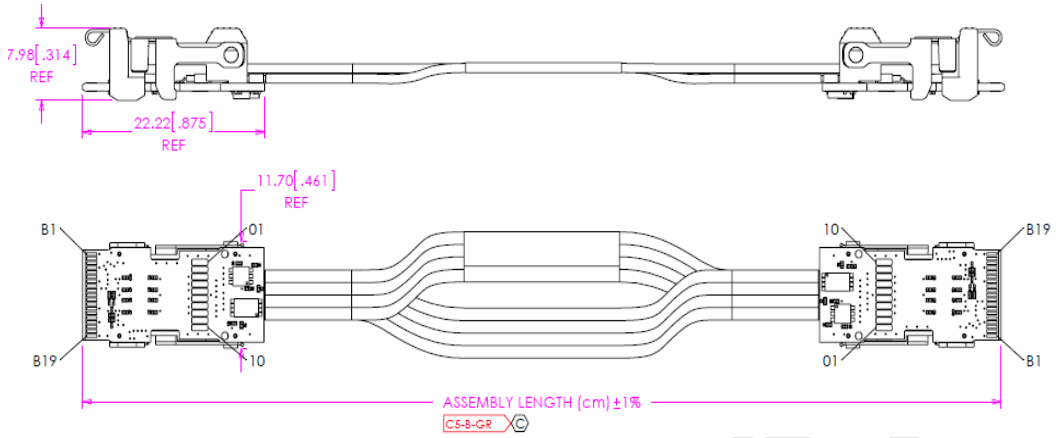


Figure 7: Dimensions of an ECUE Copper Cable

1.5.2 Optics Cable

Please contact FireFly@Samtec.com for the mechanical drawing of pin fin heat sink of the x4 25Gbps Firefly.

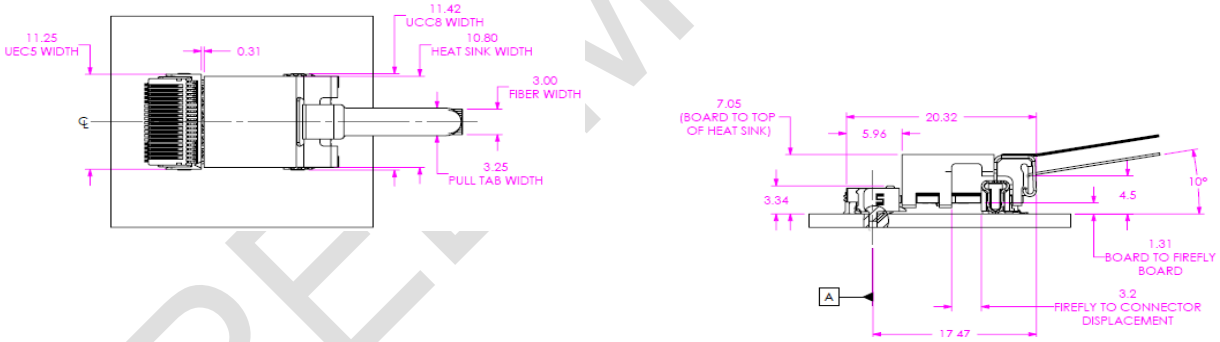


Figure 8: Dimensions of an ETUO with Flat Heat Sink

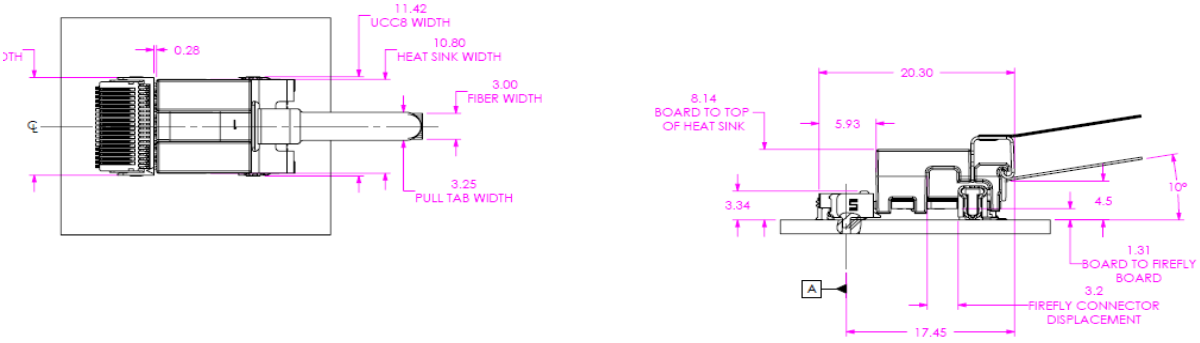


Figure 9: Dimensions of an ETUO with Flat with 3-Ribbon Pass-Through Heat Sink

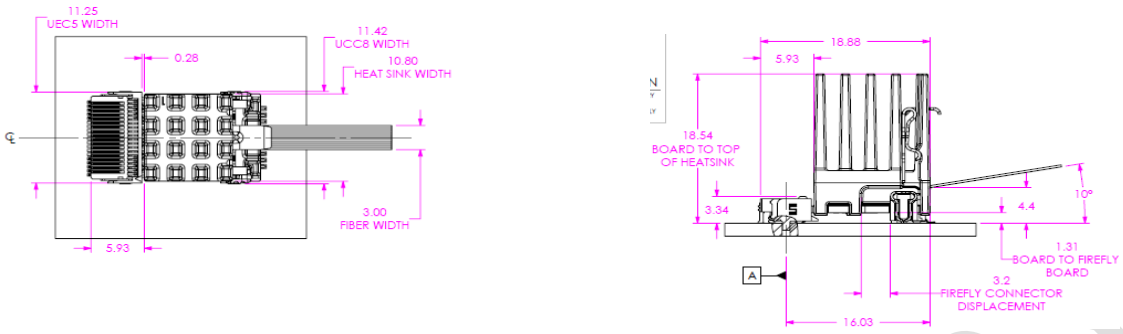


Figure 10: ETUO with Standard Pin-Fin Heat Sink

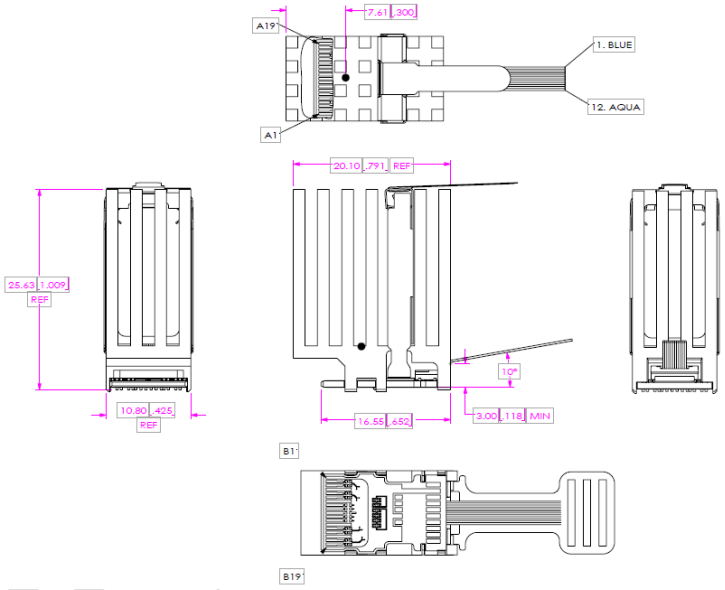


Figure 11: ETUO with High-Performance Heat Sink

1.6 *Optical Assemblies*

Optical Assemblies are available in two different configurations for the standard offering. (Note that custom assembly can also be designed, for example it is possible to have multiple ETUO-B04 going to a single 24 fiber MTP connector. Please contact FireFly@samtec.com for more information).

- Half Cable
- Active Optical Cable

The same optical engines are used in each cable. As a result, the differences are with the connectivity and not the optical engine form factor or performance. All x4 engines are duplex, that is each module has four transmit and four receive channels.

Half Cables

Figure 12: Half Cable

Half cables are available with the x4 optical engine integrated with an optical pigtail.

These assemblies are customisable to different lengths and with different fiber types, different heat sinks and different optical connectors.

Active Optical Cables

Figure 13: Active Optical Cable

Active optical cables are available with a x4 engines at each end of the cable. The transmitter of one engines are connected to the receivers at the other end and vice-versa.

These assemblies can also be configured to different lengths and with different fiber types and different heat sinks.

Y Cables

Figure 14: Y Cable

Y cables consist of two optical engines connected to a single 24 Fiber optical connector.

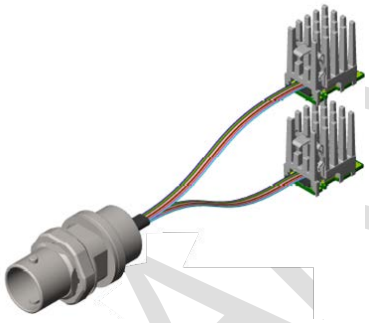
Again, these assemblies are customisable to different lengths (identical for transmit and receive) and with different fiber types, different heat sinks and different optical connectors.

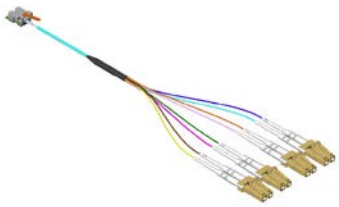
1.6.1 Optical Connector Options

The design and manufacturing process for FireFly allow for a large selection of optical connector options. Standard options are based on the MT ferrule however other options (including rugged connectors) can be manufactured as custom parts.

Some examples of possible connectors are shown below:

Two Duplex x4 module to 24F ARIB Receptacle





Duplex x4 to four duplex LC

MT38999

ARINC-801

ARINC801group

ArINC_OptikD

Figure 15: Examples of Custom Optical Connector Options

Please contact FireFly@samtec.com to discuss your requirements.

1.7 *Heat Sinks*

FireFly optical assemblies can be configured with a choice of standard or high-performance heat sinks shown in **Figure 16**. The assembly design includes an integral heatsink that is factory installed for optimum thermal performance. The module can be ordered with one of the heat sinks (described below) that support air flow cooling or cold plate cooling / heat spreaders. In additional, the FireFly design allows the use of custom heat sinks that allow the integration of cooling solutions for multiple components.

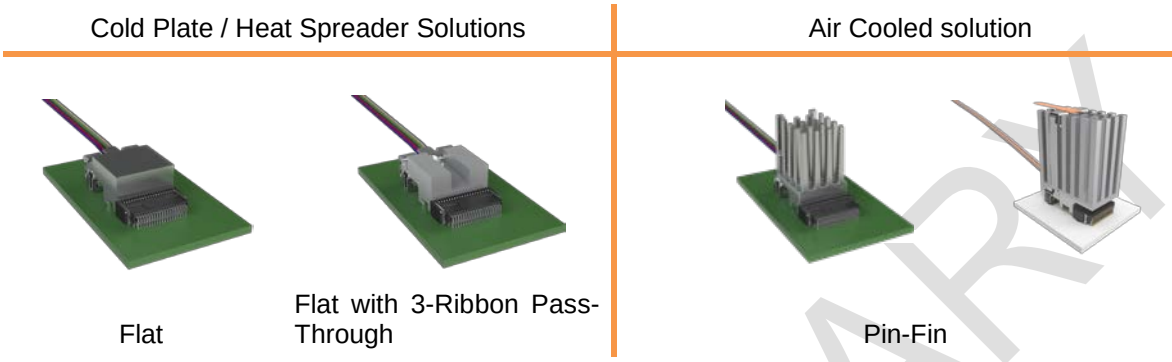


Figure 16: Heatsink Options

The *flat with 3-ribbon pass-through* heat sink is intended for ultra-high-density applications. The angled recess in the heat sink is designed to accommodate the fibers from up to three other FireFly optical assemblies configured in stacked rows. This is shown in Figure 17

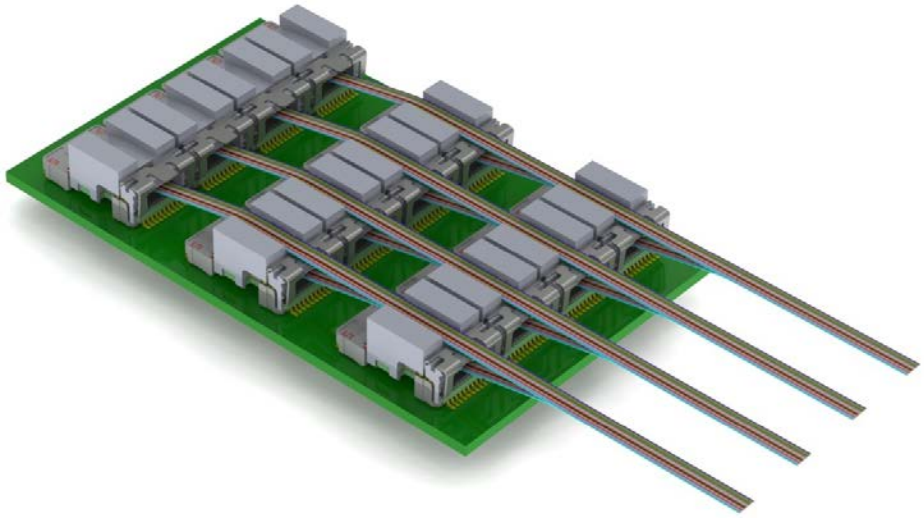
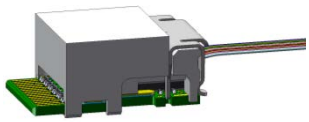


Figure 17: 4 x 3 Multi-Row FireFly Arrangement

In addition to the standard heat sinks listed, Samtec can work with customers to create heat sinks optimised for their specific designs. For further information, please contact firefly@samtec.com.

1.7.1 Thermal performance

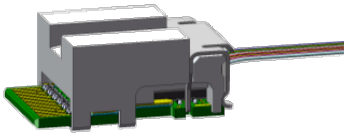
Cold Plate Cooling



-1 = Flat

Requires the use of a thermally conductive elastomer (such as FujiPoly®) between the heatsink and cold plate

Maximum compression force for cold plate attachment = 30 N



-3 = Flat with 3-ribbon pass through

Designed for use in ultra-high-density applications. The recess in the top of the heat sink is optimised to accommodate the ribbon fibers from up to three other FireFly optical assemblies without impeding the cold plate contact. An example of this configuration is shown in Figure 17.

Requires the use of a thermally conductive elastomer (such as FujiPoly®) between the heatsink and cold plate

Maximum compression force for cold plate attachment = 30 N

Air flow Cooling

-2 = Standard Pin-fin

-5 = High-Performance Pin-fin

Designed for use in high temperature applications that require air flow cooling. The pin-fin heat sink geometry is designed to provide increased surface area for heat transfer, low thermal resistance from base to fins at high airflow. It also works very well where the direction of airflow is unknown. The omnidirectional pin configuration, which allows air to enter and exit the heat sink in any direction, exposes the heat sink to the fastest possible air speed. Standard thermal tape or epoxy can be used to securely attach them to components because of their lightweight.

The required heat sink will depend on the dimensions of the bypass as well as the air temperature and bypass size.

The choice of pin-fin heat sink is a function of the inlet temperature and inlet air speed.

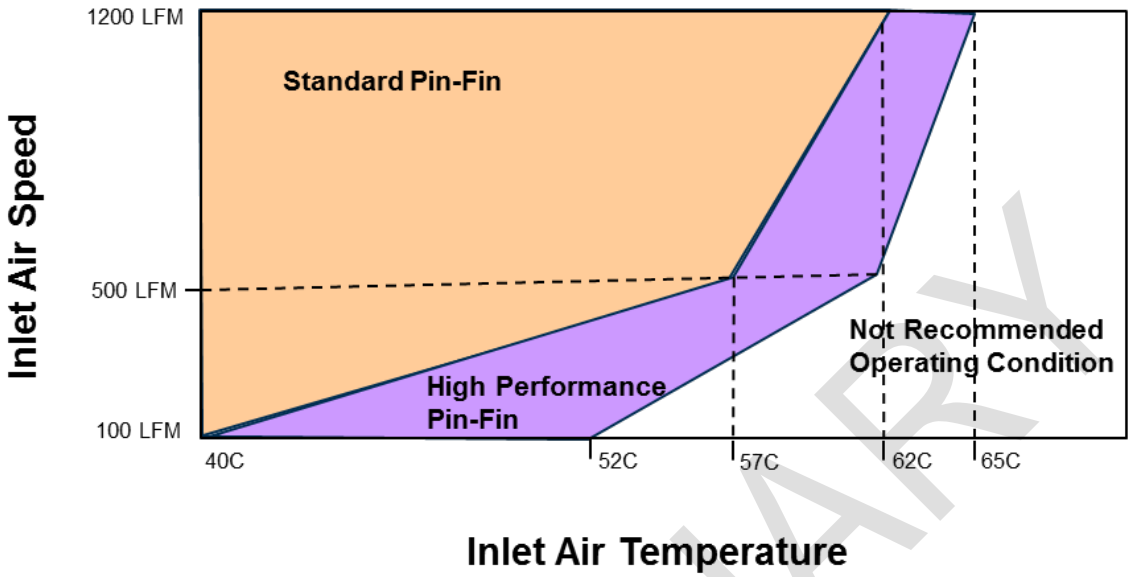
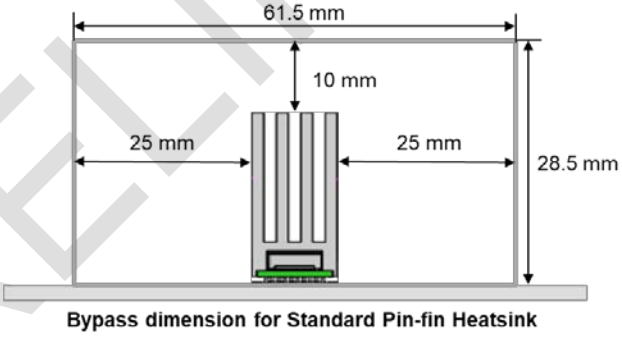
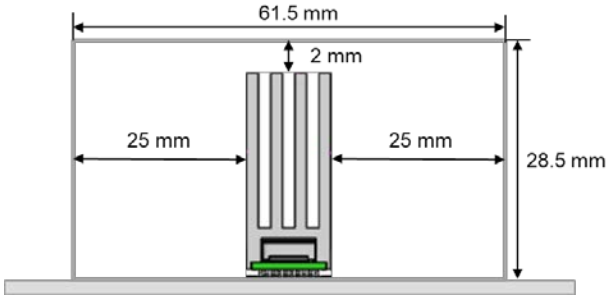


Figure 18: Airflow vs Inlet Temperature (@ 85 C Heatsink Temperature)

Figure 18 shows the chart for airflow speed versus inlet temperature required to maintain a heatsink temperature of 85 deg C, maximum. The inlet air speed will depend on the dimensions of the bypass. The above chart is based on the bypass dimensions for a standard pin-fin and high-performance pin-fin shown below:



Bypass dimension for Standard Pin-fin Heatsink



Bypass dimension for High Performance Pin-fin Heatsink

1.8 Latch

All heatsinks include a latch that locks the device into the connector set to prevent accidental removal or to prevent intermittent contact with shock or vibrations. Care should be taken to ensure that the latch is fully released (raised) before insertion or removal and that the latch is fully engaged after the part is inserted into the connector set.

1.8.1 Latch Pin

Firefly modules are shipped with a recyclable latch pin ("grenade pin") that is intended to prevent insertion of the part with the latch not fully released. This is shown both fully inserted and partially removed in Figure 19.

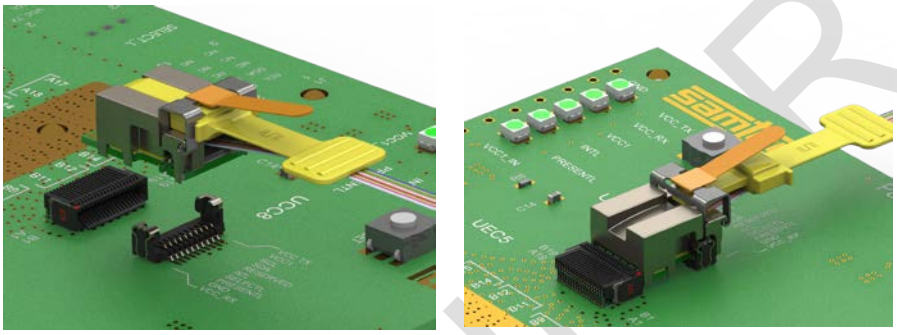


Figure 19: Heatsink with Latch Pin

1.8.2 Insertion Tool

Although the insertion process is designed to be simple, Samtec has created a tool to assist with the insertion of FireFly cold plate compatible optical assemblies. This is intended to make insertion / removal easier in applications where other components are near or access may be limited. This is designed for use with flat, grooved, or PCIe heat sinks and is shown in Figure 20. For a video describing the mating and unmating of the FireFly please consult the following video https://vimeo.com/171574689.

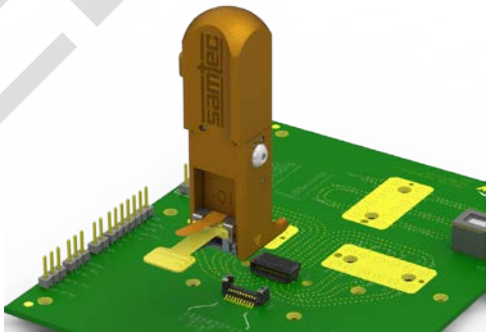


Figure 20: Insertion Tool

Please contact FireFly@samtec.com for ordering information.

An insertion tool for FireFly with pin-fin heatsinks is currently being designed.

2 On- Board Connector Specifications

2.1 *Drawings*

Mechanical dimensions and ordering information for the FireFly connectors can be found in the following location.

Mechanical dimensions of the UEC5 high speed connector can be obtained from this http://suddendocs.samtec.com/prints/uec5-xxx-2-x-d-ra-1-mkt.pdf link.

For the mechanical dimension of the UCC8 connector please follow the following link: http://suddendocs.samtec.com/prints/ucc8-xxx-x-x-x-x-a-mkt.pdf

2.2 *3D Models*

Please contact e3dmodels@samtec.com for the STEP file 3D model of the UEC5 connector.

Please follow the following link for the STEP file 3D model of the UCC8 connector: https://www.samtec.com/products/ucc8

Other formats (ACIS and IGES) can also be generated. Please contact e3dmodels@samtec.com or complete the request form available at:
http://www.samtec.com/technical-specifications/models/modelrequest.aspx

2.3 *Connector Footprints*

Detailed connector footprint information is available for the FireFly connectors and can be obtained from

http://suddendocs.samtec.com/prints/uec5-xxx-2-x-d-ra-x-footprint.pdf link. Please note that this file covers both connectors and layout design.

In addition, footprints in Allegro, Altium Designer and ASCII formats can be obtained by sending email to firefly@samtec.com.

2.4 *Mechanical*

Parameter	Units	Min	Typ	Max	Comments
Insertion Force	N		9.0		
Compression Down Force	N		30[1]		Vertical force through a cable assembly and the connector system

Table 2: Mechanical Forces

Requirement	Test Condition	Requirements	Status
Durability	EIA-364-09C	25 cycles	Pass
Contact Normal Force	EIA-364-04	30 grams minimum for gold interface	Pass

Table 3: Mechanical Specifications

2.5 *Processing Recommendations*

The following processing rules are recommended for optimal performance of the FireFly System:

- **Maximum Reflow Passes:** The parts can withstand three reflow passes at a maximum oven temperature of 260 °C.
- **Stencil Thickness:** The stencil thickness is 0.13 mm (.005")
- **Placement:** Machine placement of the parts is strongly recommended
- **Thermal Profile:** Due to the large number of processing variables (printed wiring board design, reflow oven type, component quantity, solder paste type, etc.), Samtec does not provide specific reflow profiles for any connector. We recommend that the solder paste manufacturer's guidelines be followed for optimum soldering results.
- **Reflow Environment:** Samtec recommends the use of a low-level oxygen environment (typically achieved through a nitrogen gas infusion) in the reflow process to improve solderability.
- **ROHS Compliant:** The UEC5 and UCC8 connectors are suitable for ROHS compliant processes

2.6 *Additional Resources*

For additional connector mechanical testing or product information, contact our Customer Engineering Support Group at CES@samtec.com

For additional information on high speed performance testing, contact our Signal Integrity Group at SIG@samtec.com

For additional Processing information, contact our Interconnect Processing Group at IPG@samtec.com

For ROHS, REACH or other environmental compliance information, contact our Product Environmental Compliance Group at PEC@samtec.com.

[1] Product specified to 30 N. Additional testing has demonstrated no performance degradation to 60 N.

3 Optical Assembly Specification

3.1 *Functional Description*

A functional block diagram of the engine is shown in Figure 21.

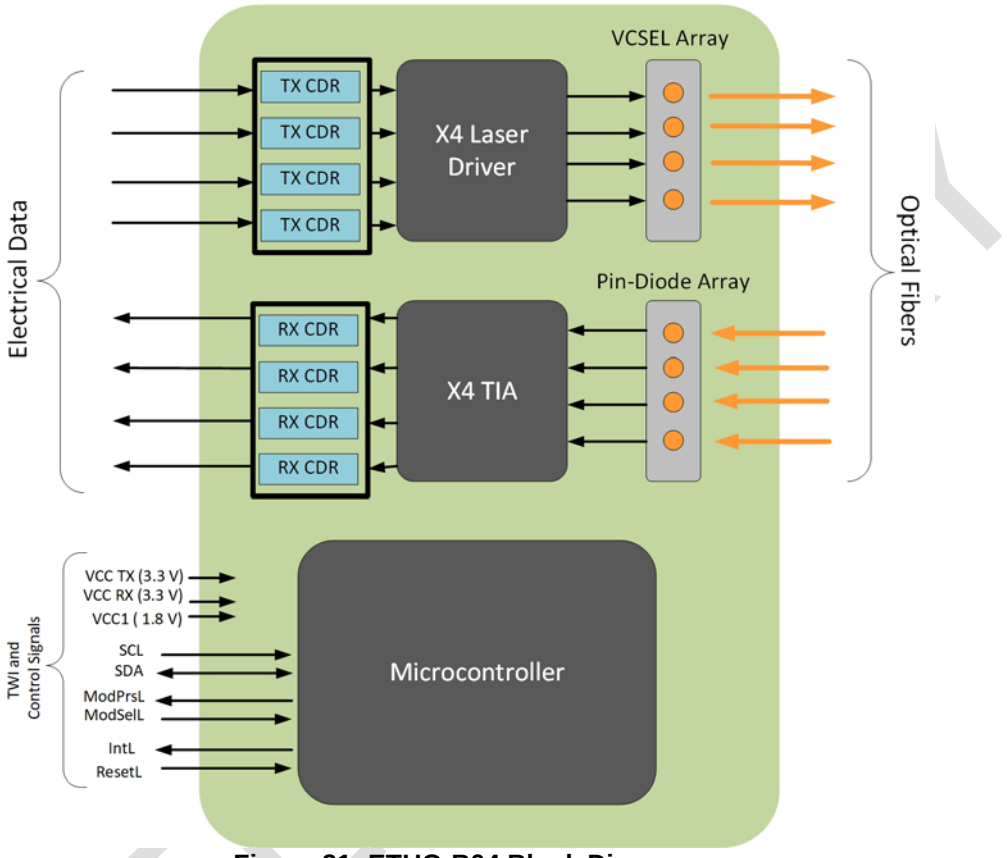


Figure 21: ETUO-B04 Block Diagram

The optical transmit portion of the engine incorporates a 4-channel VCSEL array, a 4-channel laser driver, clock data recovery, diagnostic monitors, control and bias blocks. The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 Ω. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

The optical receiver portion of the engine incorporates a 4-channel PIN photodiode array, a 4-channel TIA array, a 4-channel output buffer, clock data recovery, diagnostic monitors, control and bias blocks. The Receiver TIA provides CML compatible differential outputs for the high-speed electrical interface presenting nominal single-ended output impedances of 50 Ω to AC ground and 100 Ω differentially that should be differentially terminated with 100 Ω. Again, AC coupling capacitors are located on the optical engine and are therefore not required on the host board.

A LVTTL compatible two wire interface is provided for module control and diagnostics. Status, alarm and fault information are available via the two-wire interface. To reduce the need for polling, a hardware interrupt signal is provided to inform hosts of an assertion of an alarm.

3.2 *Absolute Maximum Specifications*

Specifications	Symbol	Unit	Min	Max	Notes
Storage Temperature		°C	-55	85	
Operating Temperature		°C	-40	85	Case Temperature
Static Discharge Voltage		V		500	Human Body model
Relative humidity		%	5	95	Non-Condensing
Supply voltage	$VCC_{3.3}$	V	-0.5	3.6	
	$VCC_{1.8}$	V	-0.5	2.00	

Table 4: Maximum Specifications

3.2.1 Link Budget

The FireFly 25G link budget is based on IEEE 802.3bm and is shown in Table 5. This assumes that OM4 fiber is used for the link and the link is 100 m or less (70 m for OM3 fiber).

Parameter	Unit	Value
Connector Loss[1]	dB	1.5
Fiber Attenuation[2]	dB	0.35
Total Loss	dB	1.85

Table 5: Link Power Budget

[1] Assumes up to 2 connection pairs each with an insertion loss of up to 0.75 dB
[2] Assumes worst case attenuation of 3.5 dB/km

3.3 *Power*

The 25G x4 ETUO module requires a 3.3 V and 1.8 V supply voltage. The 3.3 V is supplied to pins 1 and 10 and 1.8 V is supplied to pin 9 of the low speed/power connections as shown in Figure 22. The power supply specifications are listed in Table 6.

Parameter	Unit	Min	Nom	Max	Notes
$Vcc_{1.8}$	V	1.71	1.8	1.89	5% tolerance
	mA		500	700	All 8 CDRs enabled
			250		All 8 CDRs disabled
$Vcc_{3.3}$	V	3.135	3.3	3.465	5% tolerance
	mA		250	350	
Power Supply Noise Ripple ($VCC_{1.8}$ and VCC_{3_3})	mV			50	1 kHz to 10.3 GHz Measured at host.
Current Ramp rate	mA/µs			100	
UCC8 Connector Steady State Current	A			0.7	spread evenly between power pins
Power Consumption for a Firefly	W		1.7	2.5	Power consumption depends on the receiver setting. Max assumes the worst-case configuration.

Table 6: Low Speed and Power Specifications

The power filtering circuit shown in Figure 22 or an equivalent should be used to power FireFly optical assemblies.

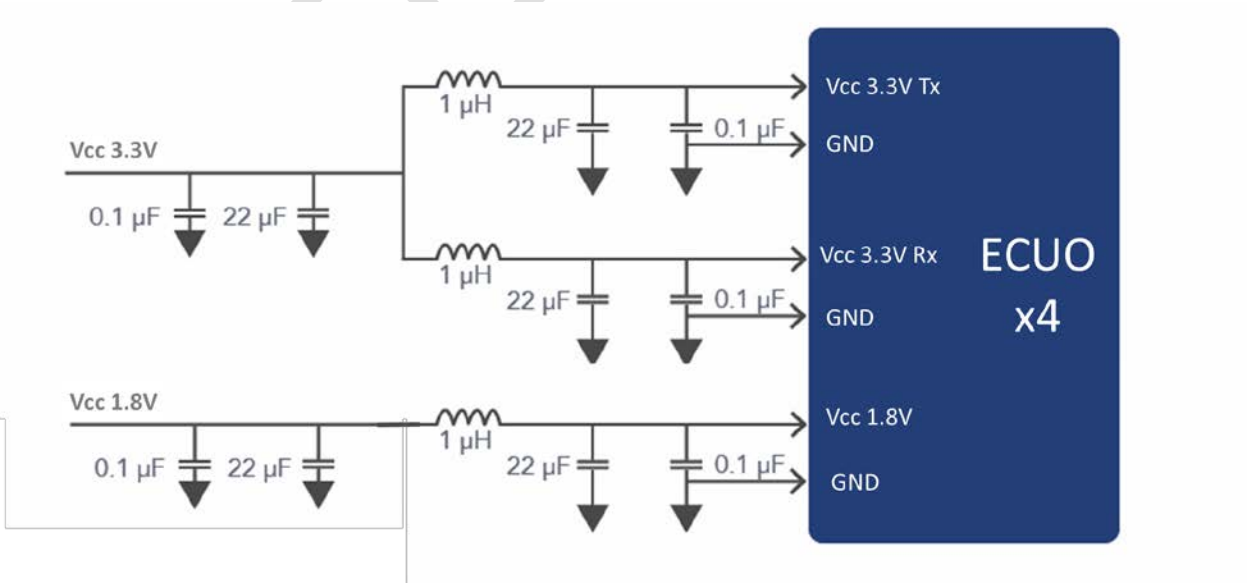


Figure 22: Recommended Power Filtering

The optical assemblies are **not hot pluggable** and should be fully installed in the connectors before power is applied.

The CDR chipsets within the part have power on sequencing requirements as shown in Figure 23.

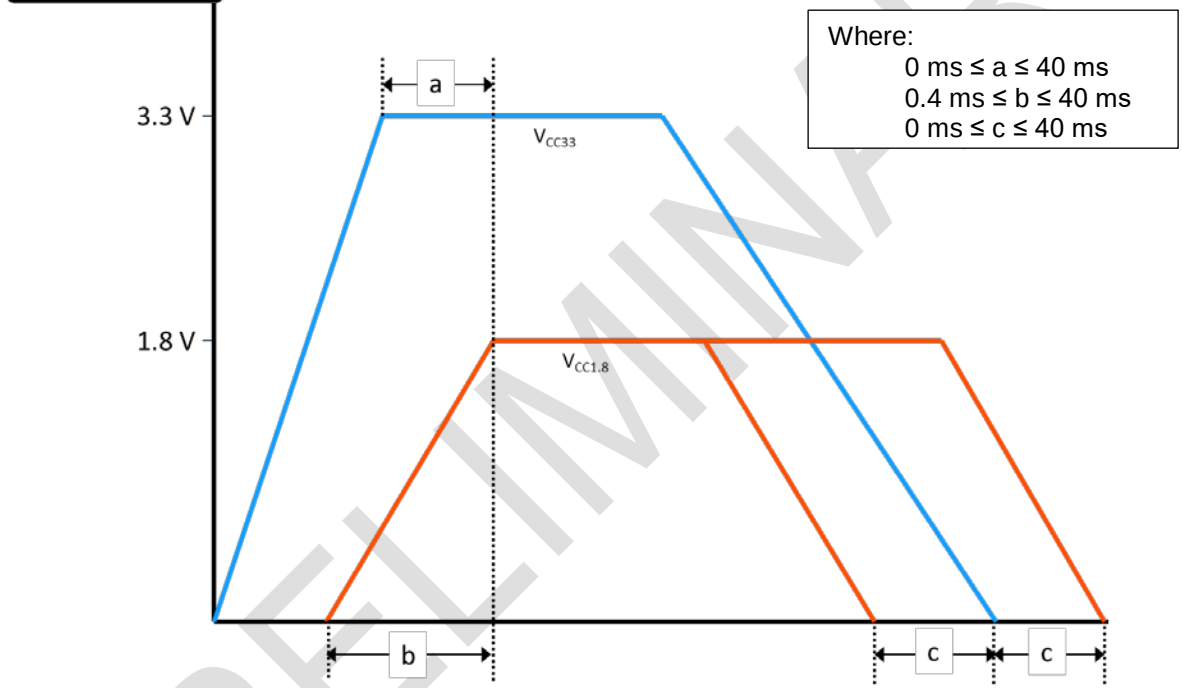


Figure 23: Power Sequence

3.4 *CDR Range*

The CDR within the 25Gx4 FireFly is limited to data rates within the following range

- 25G Retimed Mode: 25.5 ≤ f ≤ 26.0 GHz (default)

Any of the CDRs may be bypassed through an I2C write to the memory map. With the CDRs bypassed, the operational frequency range is 1 Gbps to 26.0 Gbps. It is recommended not to run the part at 25G with CDRs bypassed.

Samtec can configure parts to operate at the 25G retimed mode by default, or to turn off the CDR. Please contact firefly@samtec.com for further information.

3.5 *Protocols Supported*

FireFly 25G x4 optical assemblies support the common data center protocols that have been standardised to work over optics:

- Ethernet
- InfiniBand
- Fiber Channel

Firefly is electrically interoperable with devices that follow the Ethernet 100 GbE standard and InfiniBand EDR standards, which includes CAUI-4 and CPPI-4. Optically, FireFly operates at 850 nm and is interoperable with transceivers that follow the 100G GBASE-SR4 standard, including SFP28 and QSFP28 modules. It is also interoperable with devices that support the EDR InfiniBand standard.

Other protocols will generally work as well when the following conditions are met:

- Maximum data rate is below 26 Gbps
- Balanced Signal (i.e. equal number of 1s and 0s)
- Continuous data transmission (i.e. idle packets are required)

4 25G High Speed Performance

4.1 *25.78125 Gbps Optical Characteristics*

Parameter		Unit	Min	Nom	Max	Notes
Signalling Rate		Gbps	25.5	25.78	26.0	
Wavelength		nm	840		860	
Optical Modulation Amplitude		dBm	-4.0		3	Worst case end of life values
Average Launched Power	**(AOP)**	dBm			2.4	Worst case end of life values
Extinction Ratio		dB	3			
Relative Intensity Noise		dB/Hz		-128		
Receiver Sensitivity	**(OMA)**	dBm			-7.0	BER ≤ 10^{-12}
Receiver Overload	**(AOP)**	dBm			2.4	Overload

Table 7: 25G Optical Specification

4.2 *Electrical Specifications*

The electrical specification of a link consisting of ETUO-B04-25 connected to another ETUO-B04-25 receiver through 100 m of OM4 multi-mode fiber is described in Table 8.

Specifications	Symbol	Unit	Min	Max	Notes
Data Rate per Channel		Gbps	1	26.0	
Differential Input Amplitude	V_{DI}	mV	250	800	Peak-to-peak differential
Input Single-ended Voltage		V	-0.3	3.8	
Differential Mode Return Loss	S_{DD}	dB		See Note 1	50 MHz to 28.05 GHz[1]
Common Mode to Differential Return Loss for Tx Pin	S_{CD12}	dB		See Note 2	50 MHz to 28.05 GHz[2]
Common Mode to Differential Return Loss for Rx Pin	S_{CD21}	dB		See Note 3	50 MHz to 28.05 GHz[3]

Table 8: Transceiver Electrical Specifications

[1] Maximum S_{DD} is defined by the formula:

0.05 < f <4 GHz $\quad -11$

4 ≤ f < 28.05 GHz $\quad -6 + 9.2 \log_{10}\left(\frac{f}{14.025}\right)$

[2] Maximum S_{DC11}, S_{CD11} is defined by the formula:

0.05 < f <14 GHz $\quad -22 + 1/2\,f$

14 < f < 28.05 GHz $\quad -18 + 3/14\,f$

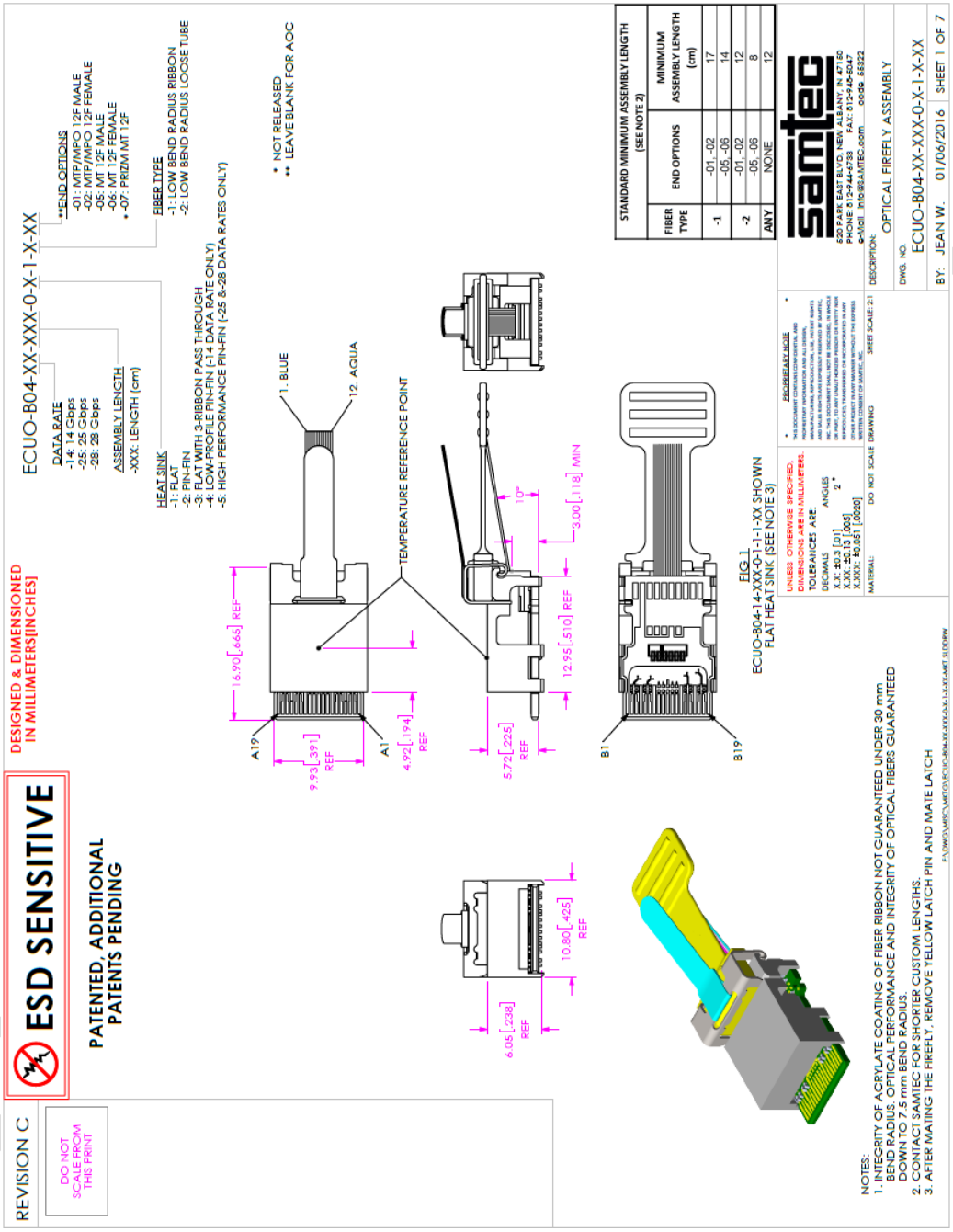
[3] Maximum S_{DC22}, S_{CD22} is defined by the formula:

0.05 < f <14 GHz $\quad -25 + 5/7\,f$

14 < f < 28.05 GHz $\quad -18 + 3/14\,f$

5 FireFly Optical - Mechanical

Please contact firefly@samtec.com for mechanical information for the Firefly 25G x4.



Three dimensional models are also available by contacting e3DModels@Samtec.com.

6 Optical Terminations

6.1 *Introduction*

The standard optical connector options available for the FireFly optical assembly are shown in Table 9 .

Option	Connector
-01	MTP® 12F Male
-02	MTP® 12F Female
-05	MT 12F Male
-06	MT 12F Female

Table 9: Optical Connector Options for FireFly Optical Assemblies

Figure 24: 12F Female MT Ferrule Connectors

For a MT connector, a cut out indicates the “top” of the connector and Pin 1 is indicated by the letter “M” on the top of the connector on the fiber side of the connector

The MTP Connector adds an additional housing around the MT ferrule. This housing provides keying to help with the correct orientation. This is shown in Figure 26.

Figure 25: 12F MTP Connector with Keying Feature Highlighted

This key is used as a reference to number the fibers and can be oriented either way (this does not affect performance). Note, Samtec FireFly optical assemblies are only offered in one configuration as standard. This configuration is based on the QSFP standard.

This standard orientation is based on the following fiber numbering convention:

- With the key up, start with the top left hand fiber and number this 1
- Count sequentially from left to right
- If there is a second row, move down to second row and continue counting at the left hand fiber
- Again, count sequentially form left to right

Examples for a 12F connector are shown in Figure 26.

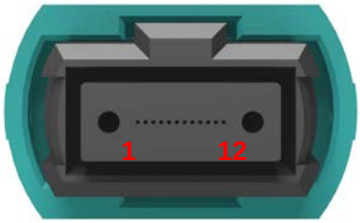


Figure 26: Fiber Numbering Convention for 12F

If the alternate configuration is required, please contact Samtec for availability.

MTP® connector has several features

- Ability to rework and re-polish the MT ferrule
- Change the gender after assembly or in the field
- Ferrule float which allows mated connectors to maintain physical contact while under an increased load.
- The use of elliptical guide pin tips reduces guide hole wear which increases the number of mate/de-mate cycles

6.2 *Prizm MT*

The Prizm MT connector is dimensionally the same as the standard MT ferrule, but will not require a physical contact of each fiber tip with its pair from the second connector for a low loss connection. Instead, micro lenses are situated in a recess of each tip that collimates an existing signal or captures an incoming signal.

6.3 *MT / MTP Performance*

The specifications for MT ferrule and MTP connectors are listed in Table 10.

Specifications	Unit	Min	Max
Insertion Loss	dB		0.75
Back Reflection	dB		20
Number of Insertions		500[1]	

Table 10: MT and MTP Specifications

6.4 *Connector Cleaning*

It is important to always clean and inspect connectors prior to connection due to the physical contact between the fibers. Dirt can prevent the fibers from contacting correctly (resulting in increased loss), block the light (increased loss) or physically damage the fiber (scratches or pits). All of these can result in increased loss and performance degradation with the optical links. See Section 15 (Appendix II) for more information.

6.5 *Fiber*

FireFly optical assemblies are available with different types of fiber. These can provide advantages when trying to route the fiber inside the box due to the form factor (loose tubed fibers will bend in all axes unlike the ribbon fiber) and minimum bend radius (see Table 11).

Firefly optical assembly is only available with OM3 pigtail. An OM3 patch cable up to 70 m and OM4 patch cable up to 100 m is supported.

Option	Description	Min Bend Radius[2] (mm)
-1	OM3 Low Bend Radius Ribbon	7.5
-2	OM3 Low Bend Radius Loose Tube	7.5
-3	Full Ribbon	7.5
-4	OM3 Low Bend Radius Loose Tube with boot	7.5

Table 11: Minimum Bend Radius

[1] The connector is compliant to the MPO specification. It is best practice to clean before every mating. Failing to do so can result in fiber damage, ferrule damage, or debris build-up inside the guide in holes, all of which impact connector performance.

[2] Integrity of acrylate coating of fiber ribbon not guaranteed under 30 mm bend radius. Optical performance and integrity of optical fibers guaranteed down to 7.5 mm bend radius.

6.5.1 Specifications

For all standard fiber options, the performance specifications are listed in Table 12

Specifications	Unit	Min	Max
Mechanical			
Core Diameter	µm	47.5	52.5
Core Non-Circularity	%	-5	5
Cladding Diameter	µm	124	126
Cladding Non-Circularity	%	-1	1
Tensile Strength3	kpsi	100	
Optical			
Modal Bandwidth	MHz.km	1500	
Numerical Aperture		0.185	0.215
Attenuation	dB/km		2.3

Table 12: OM3 Fiber Specifications

6.5.2 Strain Relief

Ribbon fibers for option -1 are singulated to a length of 7.5 cm from the FireFly heat sink to provide strain relief.

6.5.3 Assembly Length

Standard FireFly optical assemblies can be ordered in increments of 1 cm. The minimum length for standard manufacturing assemblies is shown in Table 21 and the maximum length is 999 cm.

Connector	Minimum Length (cm)		Maximum Length (cm)
	Ribbon	Loose Tube	
AOC	12	12	999
-01 MTP 12F Male	17	12	999
-02 MTP 12F Female	17	12	999
-03 MPO 12F Male	17	12	999
-04 MPO 12F Female	17	12	999
-05 MT 12F Male	14	8	999
-06 MT 12F Female	14	8	999

Table 13: FireFly Optical Minimum Assembly Lengths

The assembly length is specified to be accurate to the larger of ± 1.6 mm or ± 1%

For non-standard lengths (including the possibility of shorter lengths other than those listed in Table 13: FireFly Optical Minimum Assembly Lengths) or other custom configurations, please contact FireFly@samtec.com to discuss your requirements.

7 On Board Connector Pin Out

7.1 *Electrical Connector Pin Outs*

A simplified foot print showing pin numbers (when viewed from the top) is shown in Figure 27. Please see section 2.3 for detailed footprints of the Firefly connectors.

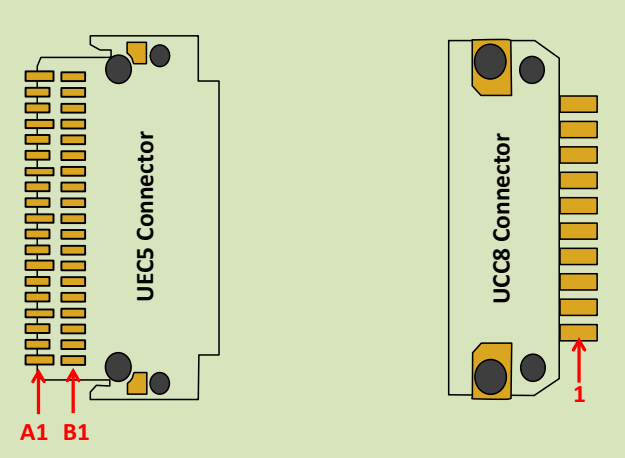


Figure 27: FireFly Connector Pin Numbering

7.2 *UCC8 Connector Pin Out*

Standard ECUE copper assemblies do not use the UCC8 connector for electrical connections. FireFly Optical assemblies require these connections which are defined in Table 14.

Pin	Description	Symbol	Notes
1	Voltage 3.3V	VCC_3.3V_Tx	3.3V supply (required)
2	Ground	GND	Signal and Heatsink Ground
3	Module Present	PRESENTL	Output, pulled low to ground when assembly is present
4	Module Select	SELECTL	Input, requires pulled low to ground when I2C read / writes are used
5	Interrupt	INTL	Output pulled low to indicate a fault condition. Remains low until latched alarms are cleared. If fault conditions persist, INTL will be pulled low after the read.
6	Reset	ResetL	If pulled low for more than 200 µs, will initiate a firmware reset and all settings will revert to default values
7	I2C Data	SDA	I2C interface data lane (input and output)
8	I2C Clock	SCL	I2C interface clock lane (input and output)
9	Voltage 1.8V	Vcc_1.8V	1.8 V supply (required when using part with CDR)
10	Voltage 3.3V	Vcc_3.3_Rx	3.3 V supply (required)

Table 14: UCC8 Pin Out

PresentL (Pin 3)

The Module Present Pin is an output contact and is tied directly to ground inside the FireFly optical assembly.

The PresentL pin is used to indicate to the host that the FireFly connector is populated. In the absence of a FireFly optical assembly, this should be pulled up to the host Vcc. When the optical assembly is inserted, it completes the path to ground and pulls PRESENTL to a low state/

ModSelL (Pin 4)

The module select is an input contact and is biased to the “High” state inside the FireFly optical assembly.

The ModSelL pin allows multiple FireFly optical assemblies to be on a standard I2C Serial bus. By default, this pin is held low by the host. When in this state, the module will respond to writes and queries on the I2C interface. When the ModSelL pin is pulled high by the host, the optical assembly does not respond to or acknowledge any I2C query or command.

IntL (Pin 5)

IntL is an output contact. When low, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the two-wire serial interface. The IntL contact is an open collector output and should be pulled to 3.3 V on the host board.

Reset (Pin 6)

The ResetL contact is pulled to Vcc inside the FireFly with a 24 kΩ pull up resistor. A low level on the ResetL pin for more than 200 μs initiates a complete module reset, returning all user settings to their default state. During the execution of a reset, the host shall ignore all status bits until optical engine indicates a completion of the reset interrupts. This is indicated by the engine asserting “low” on the IntL pin with the Data_Not_Ready bit (Lower00 Byte6 bit 0) negated.

Note, operation is not assumed when the Reset pin is pulled low and so electrical and optical performance is not guaranteed.

Figure 28 shows the schematic implementation of the UCC8 connector. Pullup resistances are needed on the host board for INTL, SDA and SCL. The recommended value for the pullup resistance for the INTL is R=3.3 kΩ. For SDA and SCL the pullup resistance value necessary will depend on the number of devices connected to the I2C bus. A typical value of Rp=3.3 kΩ will usually be appropriate.

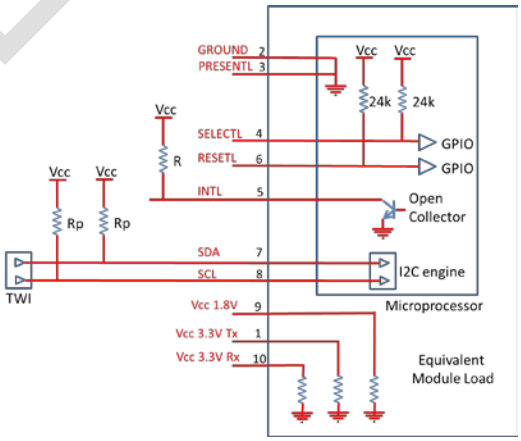


Figure 28: Schematic of the Implementation of UCC8 Connection for the ETUO

7.3 *UEC5 Connector Pin Out*

The electrical pin out for the ETUO optical assemblies is shown in Table 15.

ETUO		
Pin Number	Row A	Row B
1	GND	GND
2	Tx 1N	Tx 2N
3	Tx 1P	Tx 2P
4	GND	GND
5	Tx 3N	Tx 4N
6	Tx 3P	Tx 4P
7	GND	GND
8	Reserved[1]	Reserved
9	Reserved	Reserved
10	Reserved	Reserved
11	Reserved	Reserved
12	Reserved	Reserved
13	GND	GND
14	Rx 4P	Rx 3P
15	Rx 4N	Rx 3N
16	GND	GND
17	Rx 2P	Rx 1P
18	Rx 2N	Rx 1N
19	GND	GND

Table 15: UEC5 Pin Out For ETUO Optical Assemblies

The electrical pin out for the ETUO optical assembly paddle board is as per Figure 29.

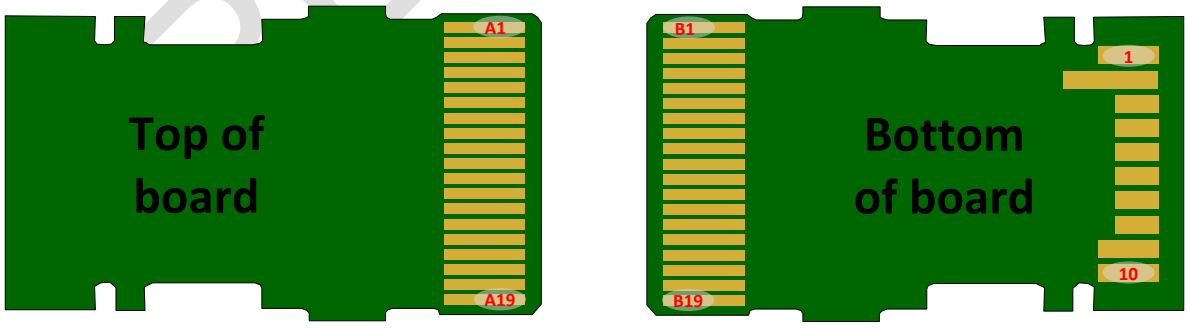


Figure 29: ETUO Pin Out

[1] Pin 8 through 12 should be connected to ground with a 50 Ω resistance for best performance.

8 Optical Connector Pin Out

The ETUO-B04 uses a 12 fiber MT, MPO or MTP connector. The connector pin out for the optical assembly is shown in Table 16. The colour corresponding to each fiber is also listed for reference.

Fiber Number	Function	Fiber Color
1	Rx 1	Dark Blue
2	Rx 2	Orange
3	Rx 3	Green
4	Rx 4	Brown
5	-	Slate
6	-	White
7	-	Red
8	-	Black
9	Tx 4	Yellow
10	Tx 3	Violet
11	Tx 2	Rose
12	Tx 1	Aqua

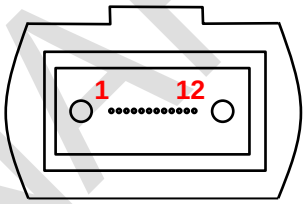


Table 16: ETUO-B04 Optical Connector Pin Out

Note, 8 fibers optical cable may be used instead of the 12 fiber shown above. Dark fibers (numbered 5-8) shown in Table 16 may not exist.

9 Compliance and Regulatory

Samtec manufactures in accordance with the following guidelines, in order of precedence:

- Samtec Workmanship Guideline & Boundary Documents
- IPC-A-610F Class 2
- IEC61300-3-35

9.1 *Environmental Compliance*

The ETUO and ECUE series meet the requirements of the following environmental compliance:

Designation	Description
RoHS	Free of Intentionally added lead
EU REACH	European Union REACH Regulation EC 1907/200g and ECHA SVHC Candidate List
EU RoHS2	European Union Directive 2011/65/EU including compliance with the Annex annulment of the deca-BDE exemption
China RoHs	Compliant per the "Management Methods for Controlling Pollution by Electronic Information Products" Law
WEEE	European Community directive 2002/96/EC on waste electrical and electronic equipment

Table 17: Environmental Compliance

Note: Product environmental disclosure is not to be construed as a warranty or quality specification. Environmental regulatory information is for guidance purposes only. Product users are responsible for determining the applicability of legislation and regulations based on their individual usage of the product.

Further information can be found at:
http://suddendocs.samtec.com/standard_products/environmental_compliance/web_compliant_matrix.pdf

9.2 *Laser Eye Safety*

When used with MT/MPO/MTP optical connectors, the ETUO series is classified as a Class 1 laser.

Complies with FDA performance standards for laser products except for deviations pursuant to Laser Notice No. 50, dated June 24, 2007.

Caution – Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Manufacturing Location: Samtec, 520 Park East Blvd., New Albany, IN 47150.

The Class 1 Laser Product designation is only for the FireFly.

The laser classification of the end system is independent of the FireFly classification and should be certified as the end system classification can be higher (or lower) than that of the FireFly.

ETUO	-	B04	-	Data Rate	-	Cable Length	-	0	-	Heat Sink	-	1	-	Fiber Type	-	End 2 Options
				-25 = x4 25G		-XXX = Length (cm)				-1 = Flat -2 = Pin-Fin -3 = Flat with 3-ribbon pass through -5 = High Performance Pin Fin				-1 = Low bend radius ribbon -2 = Low bend radius loose tube -3 = Low bend radius loose tube -4 = Low bend radius loose tube		Leave blank for full AOC -01 = MTP® 12F Male -02 = MTP® 12F Female -05 = MT 12F Male -06 = MT 12F Female

10 Ordering Information

10.1 *ETUO*

10.2 *UEC5-2 Connector*

UEC5	-	019	-	2	-	H	-	D	-	RA	-	Weld Tab Style	-	A
												-1 = Thru-hole -2= Surface Mount		

10.3 *UCC8 Connector*

UCC8	-	010	-	1	-	H	-	S	-	Weld Tab	-	A
										-1= Through-hole -2 = Surface Mount		

11 Fiber Connectivity

Care should be taken when interconnecting ETUO optical assemblies to preserve lane numbering assignments. Detailed information about the connectivity of the ETUO x4 28G can be found in FireFly Optical Half Cables Application Note.

For the Tx1 transmitter to map to the Rx1 receiver there must be no inversion in the fiber link. Figure 30 shows the connectivity when two ETUO-B04 are connected directly using an aligned MPO adaptor.

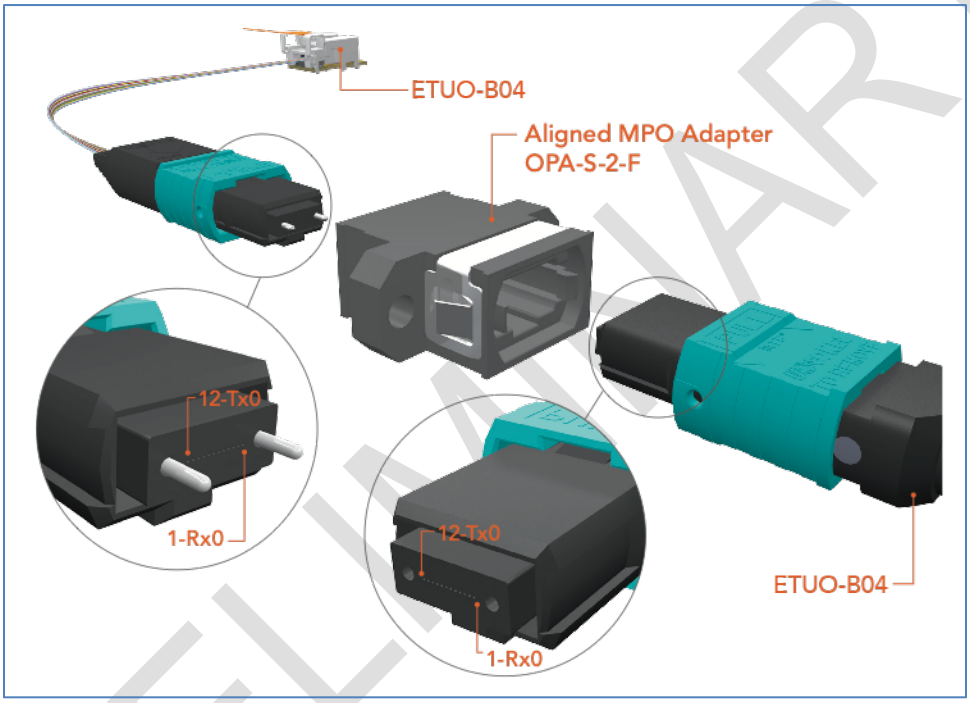


Figure 30: ETU0-B04 to ETUO-B04 Fiber Connectivity

Figure 31 shows the connection of two ETUO-B04 half cable via a FOPC patchcord. Two opposed MPO connector adaptors are used to have the proper connection. (note that two aligned MPO would also work properly)

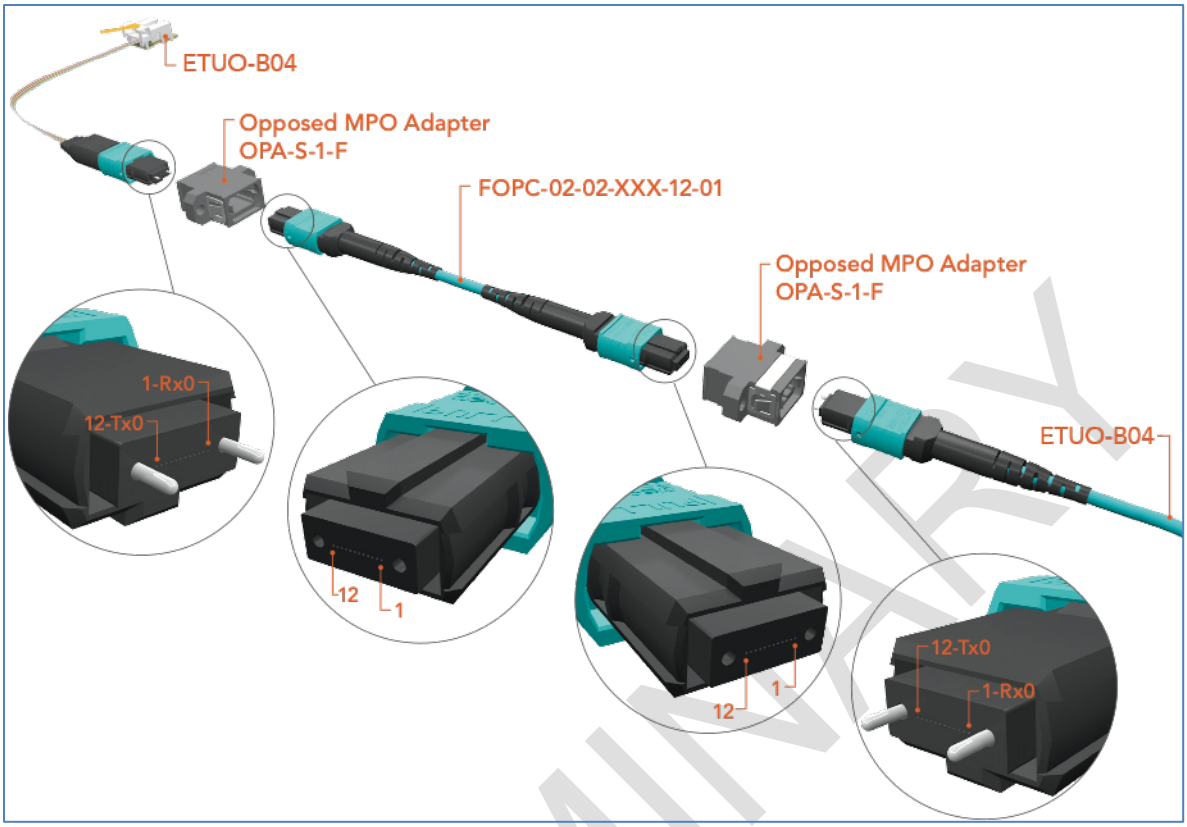


Figure 31: Connection of a ETUO-B04 to a ETUO-B04 Using an FOPC

Figure 32 shows the fiber connectivity to connect a ETUO-B04 to a QSFP+ via a FOPC. The end connection of the FOPC can connect directly into a QSFP+ type of module with MPO connectivity.

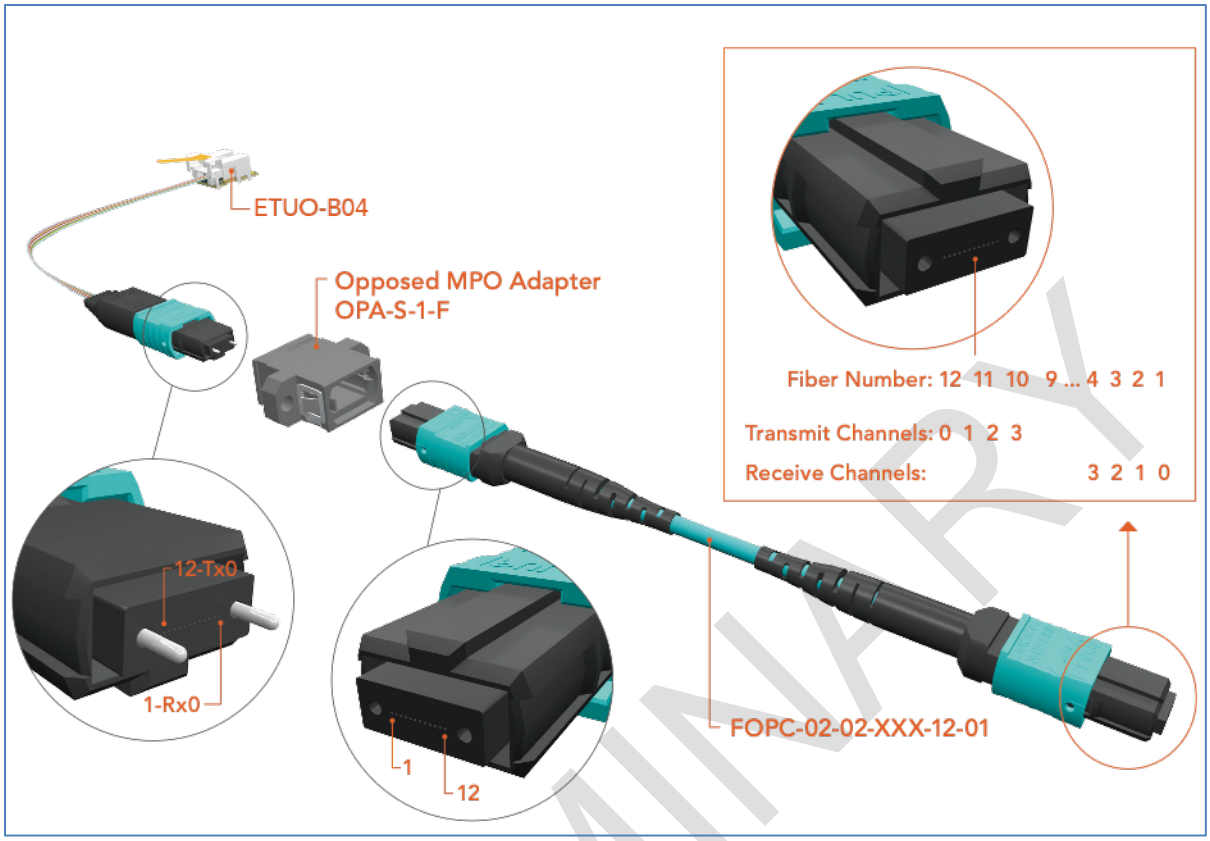


Figure 32: Connection of a ETUO-B04 to a QSFP+ Using an FOPC

12 Firmware Upgrade

FireFly Optical Assemblies are capable of being their firmware updated in-situ on the host. Please contact FireFly@samtec.com for further information on the protocol used.

13 Control and Memory Map

13.1 *Control*

A management interface is provided based on an industry standard two-wire serial interface scaled for 3.3 V LVTTL. The specification has been modelled on the definition of the QSFP (SFF-8636) with additional features to enable advanced functionality.

The specification provides a fixed address for the ETUO-B04. The address is shown in Table 18.

End	7-bit Address	8-bit address	
		Write	Read
Transmit/Receiver	0x50	0xA0	0xA1

Table 18: I2C Addressing

Samtec has extended this to allow the capability to reconfigure the address to prevent bus conflicts with other components on the bus or to simplify communication with multiple FireFly on a bus. This achieved by programming byte 255 of Upper02. In addition, a part can be configured to respond to both the original address and a new address. This is demonstrated for the transmitter in Table 19.

Upper02 Byte 255	Function
0x00	Will respond to a general call and address 0x50 if ModSelL is low Will not respond if ModSelL is high
0x01 – 0x7E	Will respond to matched address if ModSelL is low Will not respond if ModSelL is high
0x7F – 0xFF	Will respond to address 0x50 if ModSelL is low Will not respond if ModSelL is high

Table 19: Programmable Address Functionality

Care must be taken to ensure that the ModSelL pin is used to toggle control of different modules when required by the value chosen. In addition, the assert and de-assert times must be considered to prevent communication conflicts.

13.1.1 Voltage and Timing Specification

Management Interface Voltage Specification

Management signalling logic levels are based on Low Voltage CMOS operating at 3.3 V Vcc. The host should use a pull-up to $VCC_{3.3}$ for the two-wire interface SCL (clock), SDA (address & data), and INTL/Reset_L signals. The electrical specifications are given in Table 21.

Parameter	Symbol	Min	Max	Unit
Input Voltage Low	V_{il}	-0.5	0.3* $VCC_{3.3}$	V
Input Voltage High	V_{ih}	0.7* $VCC_{3.3}$	3.6	V
Output Voltage Low	V_{ol}	0	0.4	V
Output Voltage High	V_{oh}	2.6	$VCC_{3.3}$ - 0.3	V
Input Current	I_I	-10	10	µA
Capacitance on SCL and SDA contacts	Ci,SCLSDA		10	pF
Capacitance on INTL/Reset_L I/O contacts	Ci,INTL		10	pF
Total Bus capacitive load	C_b		28	pF

Table 20: Low Speed Control and Sense Signal Specifications

Management Interface Timing specification

In order to support a multi-lane device a 400 kHz clock rate for the serial interface is expected. The timing requirements are shown in Figure 33 and specified in Table 20. All values are referred to V_{ih}(min) and V_{il}(max) levels shown in Table 21.

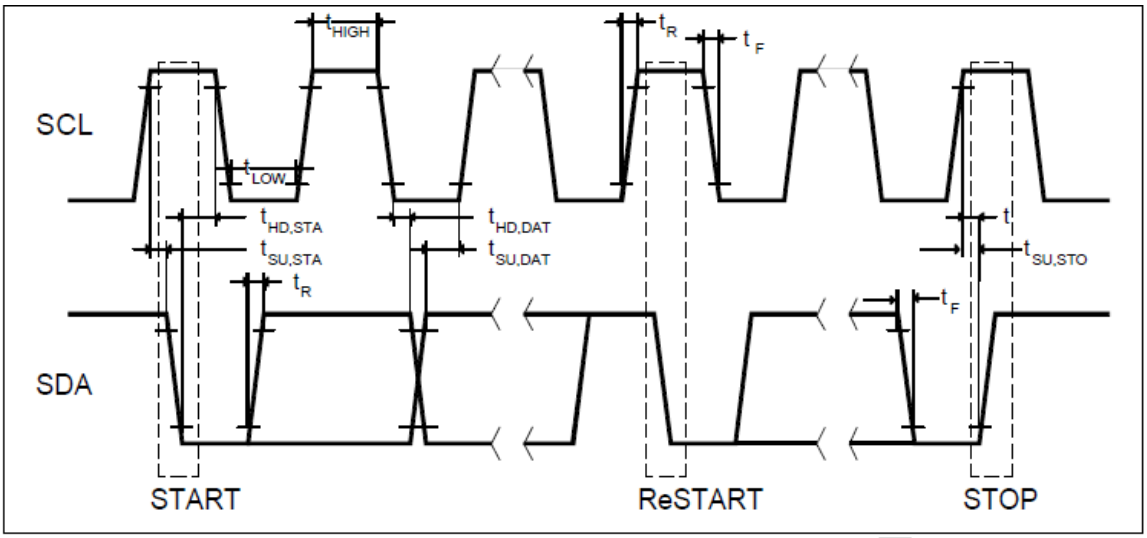


Figure 33: Management Interface Two Wire Serial Interface Timing Diagram

Parameter	Symbol	Min	Max	Unit	Condition
Clock Frequency	f_{SCL}	0	400	kHz	
Clock Pulse Width Low	t_{LOW}	1.3		µs	
Clock Pulse Width High	t_{HIGH}	0.6		µs	
Time bus free before new transmission can start	t_{BUF}	1.3		µs	1
START Set-up Time	$t_{SU,STA}$	0.6		µs	
START Hold Time	$t_{HD,STA}$	0.6		µs	
Data Set-up Time	$t_{SU,DAT}$	0.1		µs	2
Data Hold Time	$t_{HD,DAT}$	0	3.45	µs	3
SDA and SCL rise time	t_R,400	20	300	ns	4
SDA and SCL fall time	t_F,400	20	250	ns	5
STOP Set-up Time	$t_{SU,STO}$	0.6		µs	
ModSelL Set-up Time	$t_{host\_select\_setup}$	2		ms	6
ModSelL Hold Time	$t_{host\_select\_hold}$	10		µs	7
ModSelL Release Time	$T_{host\_release}$	10		µs	8
ModSelL Aborted sequence - bus release	$t_{deselect\_abort}$	2		ms	9

Table 21: Management Interface Two Wire Serial Interface Timing Diagram Specifications

1. Between STOP & START and between ACK & ReSTART.
2. Data in Set UP Time is measured from V_{il}(max)SDA or V_{ih}(max)SCL.
3. Data in Hold Time is measured from V_{il}(max)SCL or V_{ih}(max)SDA or V_{ih}(min)SDA.
4. Rise Time is measured from V_{ol}(max)SDA to V_{oh}(min)SDA.
5. Fall Time is measured from V_{oh}(min)SDA to V_{ol}(max)SDA.
6. Setup time on the select lines before start of a host-initiated serial bus sequence.
7. Time from ModSelL being pulled low to guaranteed response from FireFly
8. Time from last I2C interaction to ModSelL being released
9. Delay from a host de-asserting ModSelL (at any point in a bus sequence) to the optical engine no longer responding to writes/queries.

13.1.2 Memory Interaction Specifications

Non-volatile memory may be accessed in either single-byte or multiple-byte memory blocks. The minimum size write block is 1 byte and the maximum is 4 bytes.

Timing for Memory Transactions

The management interface memory transaction timings are given in Table 22: Management interface memory transaction timing specification.

Parameter	Symbol	Min	Max	Unit	Condition
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		500	µs	1,2
Complete Single or Sequential Write	t_{WR}		40	ms	3
Endurance (write cycles)		40,000		cycles	4

Table 22: Management Interface Memory Transaction Timing Specification

1. Maximum time the optical assembly may hold the SCL line low before continuing with a read or write operation.
2. Please note that when writing to the upper page 0x02 (The user writable EEPROM), the time between write sequence should be at least 40ms. If it isn't, the clock may be stretched by the optical module to 40 ms.
3. Complete up to 4 Byte write. Timing should start from Stop bit at the end of the sequential write operation and continue until the module responds to another operation.
4. 40,000 write cycles at 85 °C.

Timing for Control and Status Functions

Timing for the FireFly optical assemblies' control and status functions are described in Table 23.

Parameter	Symbol	Min	Max	Unit	Notes
Initialisation Time	tinit		2000	ms	1, 2, 3
Reset Init Assert Time	t_reset_init	200		µs	4
Monitor Data Ready Time	tdata		2	s	5
Reset Assert Time	tRSTL,OFF		2	ms	6
INTL Assert Time	tINTL,ON		200	ms	7
INTL Deassert Time	tINTL,OFF		100	ms	8
Rx LOS Assert Time	tLOS,ON		100	ms	9
Tx Fault Assert Time	tTxfault,ON		200	ms	10
Flag Assert Time	tflag,ON		200	ms	11
Mask Assert Time	tmask,OFF		100	ms	12
Mask Deassert Time	tmask,ON		100	ms	13
Page Select Wait Time, Upper Page 00, 03 or 0b	tpage_00/01_select		100	ms	14
Page Select Wait Time, Upper Page 02	tpage_02_select		600	ms	15

Table 23: I/O timing for Control and Status Functions

1. Time from power on, hot plug or rising edge of Reset until the optical assembly is fully functional.
2. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level
3. Fully functional is defined as INTL asserted due to Data Not Ready (Byte 2, bit 0) de-asserted.
4. A reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin
5. Time from power on to Data Not Ready (Byte 2, bit 0) de-asserted and INTL asserted.
6. Time from rising edge on the Reset_L contact until the Firefly optical assembly is fully functional. During the Reset Time the optical assembly will not respond to a "low" on the INTL/Reset_L signal.
7. Time from occurrence of condition triggering INTL until Vout:INTL = Vol.
8. Time from clear on read operation of associated flag until INTL Status (Lower page, byte 2, bit 1) is cleared. This includes de-assert times for Rx LOS, Tx Fault and other flag bits. Measured from falling clock edge after stop bit of read transaction.
9. Time from Rx LOS state to Rx LOS bit set (value = 1b) and INTL asserted.
10. Time from Tx Fault state to Tx Fault bit set (value = 1b) and INTL asserted.
11. Time from occurrence of condition triggering flag to associated flag bit set (value = 1b) and INTL asserted.
12. Time from mask bit set (value = 1b) until associated INTL assertion is inhibited.
13. Time from mask bit cleared (value = 0b) until associated INTL operation resumes.
14. Time from setting the Upper Page Select Byte (Lower Page Byte 127) to 0x01 from 0x00, or to 0x00 from 0x01, until the associated upper page is accessible.
15. Time from setting the Upper Page Select Byte (Lower Page Byte 127) to 0x02 or from 0x02 to either 0x00 or -x01, until the associated upper page is accessible. This longer period for Upper Page 02, vs. other Upper Pages, allows more complex memory management for this infrequently-accessed upper page.

Timing for Squelch and Disable Functions

Squelch and disable times are described in Table 24.

Parameter	Symbol	Max	Unit	Notes
Combination of Tx+Rx Squelch Assert Time	$t_{Rxsq,ON}$	90	µs	1
Combination of Tx+Rx Squelch Deassert Time	$t_{Rxsq,OFF}$	5	µs	2
Tx Channel Disable Assert Time	$t_{Txdis,ON}$	100	ms	3
Tx Channel Disable Deassert Time	$t_{Txdis,OFF}$	400	ms	4
Rx Output Disable Assert Time	$t_{Rxdis,ON}$	100	ms	5
Rx Output Disable Deassert Time	$t_{Rxdis,OFF}$	100	ms	6
Squelch Disable Assert Time	$t_{Sqdis,ON}$	100	ms	7
Squelch Disable Deassert Time	$t_{Sqdis,OFF}$	100	ms	8

Table 24: I/O Timing for Squelch and Disable

1. Time from loss of Tx input signal until the squelched output condition on the Rx is reached.
2. Time from resumption of Tx input signals until normal Rx output condition is reached.
3. Time from Tx Disable bit set until optical output falls below 10% of nominal.
4. Time from Tx Disable bit cleared until optical output rises above 90% of nominal. Measured from Stop bit low to high SDA transition.
5. Time from Rx Output Disable bit set (value = 1b) until Rx output falls below 10% of nominal.
6. Time from Rx Output Disable bit cleared (value = 0b) until Rx output rises above 90% of nominal.
7. This applies to Rx and Tx Squelch and is the time from bit set until squelch functionality is disabled
8. This applies to Rx and Tx Squelch and is the time from bit cleared) until squelch functionality is enabled.

13.1.3 Device Operation

Serial Clock (SCL): The host supplied SCL input to the engine is used to positive edge clock data into each FireFly optical assembly and negative-edge clock data out of each optical assembly. The SCL line will be pulled low by the module during clock stretching

Serial Data (SDA): The SDA signal is bidirectional for serial data transfer. This signal is open-drain or open-collector driven and may be wire-ORed with multiple open-drain or open collector devices, limited by aggregate capacitance vs. clock speed.

Master/Slave: FireFly optical assemblies operate only as slave devices. The host must provide a bus master for SCL and initiate all read/write communication.

Multiple devices per SCL/SDA: Support of multiple ports in a host is provided through the use of the ModSelL pin. This should be pulled low to enable two wire interface reads/writes.

Clock and Data Transitions: The SDA signal is normally pulled high in the host. Data on the SDA signal may change only during SCL low time periods. Data changes during SCL high periods indicate a START or STOP condition**.** All addresses and data words are serially transmitted to and from the module in 8-bit words. Every byte on the SDA line must be 8-bits long. Data is transferred with the most significant bit (MSB) first.

START Condition: A high-to-low transition of SDA with SCL high is a START condition, which must precede any other command.

STOP Condition: A low-to-high transition of SDA with SCL high is a STOP condition.

Acknowledge: After sending each 8-bit word, the transmitter releases the SDA line for one-bit time, during which the receiver can pull SDA low (zero) to acknowledge (ACK) that it has received each word. Device address bytes and write data bytes initiated by the host are acknowledged by the optical assemblies. Read data bytes transmitted by the module shall be acknowledged by the host for all but the final byte read which will be a NACK then host shall respond with a STOP.

Device Addressing: FireFly optical assemblies require an 8-bit device address word following a start condition to enable a read or write operation. The device address word consists of a mandatory sequence for the first seven most significant bits. The eighth bit of the device address is the read/write operating select bit. A read operation is initiated if this bit is set high and a write operation is initiated if this bit is set low. Upon compare of the device address the module shall output a zero (ACK) on the SDA line to acknowledge the address.

Nomenclature for all registers more than 1 bit long is MSB-LSB.

13.1.4 Read/Write Functionality

This section describes the functionality for read/write operations. Further information can be obtained from SFF-8636 Rev 2.6 specification.

Memory Access Counter (Read Operations)

FireFly optical assemblies maintain an internal data word address counter containing the last address accessed during the latest read operation, incremented by one. This address stays valid between operations as long as power is maintained. The address "roll over" during read and writes operations is from the last byte of the 128-byte memory page to the first byte of the same page.

Read Operations (Current Access Read)

A current address read operation requires only the device address read word (10100001) be sent. Once acknowledged by the FireFly optical assembly, the current address data word is serially clocked out. The host responds with an acknowledge and generates a STOP condition once the data word is read.

Read Operations (Random Read)

A random read operation requires a write operation to load in the target byte Address. This is accomplished by the following sequence:

- The target 8-bit data word address is sent following the device address write word (1010 0000) and acknowledged by the optical assembly.
- The host then generates another START (restart) condition and a current address read by sending a device read base address (1010 0001).
- The FireFly optical assembly acknowledges the device address and serially clocks out the requested data word.
- The host should generate a STOP condition once the data word is read.

Read Operations (Sequential Read)

Sequential reads are initiated by either a current address read or a random address read. To specify a sequential read, the host responds with an acknowledge (instead of a STOP) after each data word. As long as the FireFly optical assembly receives an acknowledge, it shall serially clock out sequential data words. The sequence is terminated when the host responds with a NACK and a STOP instead of an acknowledge.

Write Operations (Byte Write)

A write operation requires an 8-bit data word address following the device address write word and acknowledgement. Upon receipt of this address, the optical assembly will again respond with a zero (ACK) to acknowledge and then clock in the first 8-bit data word. Following the receipt of the 8-bit data word, the optical assembly shall output a zero (ACK) and the host master must terminate the write sequence with a STOP condition for the write cycle to complete. If a START condition is sent in place of a STOP condition (i.e. a repeated START per the two-wire interface specification) the write is aborted and the data received during that operation is discarded. Upon receipt of the proper STOP condition, the FireFly optical assembly enters an internally timed write cycle, t_{WR}, to internal memory.

The optical assembly disables its management interface input during this write cycle and shall not respond or acknowledge subsequent commands until the write is complete. Note that two-wire interface "Combined Format" using repeated START conditions is not supported on write commands.

Write Operations (Sequential Write)

FireFly optical assemblies support up to a 4-sequential byte write without repeatedly sending engine address and memory address information. A "sequential" write is initiated the same way as a single byte write, but the host master does not send a stop condition after the first word is clocked in. Instead, after the FireFly optical assembly acknowledges receipt of the first data word, the host can transmit up to three more data words. The FireFly optical assembly will send an acknowledge after each data word received. The host must terminate the sequential write sequence with a STOP condition or the write operation shall be aborted, and data discarded. Note that two-wire interface "combined format" using repeated START conditions is not supported on write.

13.2 *Memory Map*

This section defines the Memory Map for the FireFly x4 duplex optical assemblies used for serial ID, digital monitoring and control functions. The interface has been derived from the Specification for Management Interface for Cabled Environments (SFF-8636). The memory map has been modified to remove functionality that is not available within FireFly x4 optical assemblies. Paging on upper pages is used to allow slower access to less time-critical information.

The SFF-8636 specification calls for a list of cable parameters to be readable through a two-wire interface, commonly referred as the “EEPROM” parameters. When the first standard revision was written, all the parameters were static and were stored in an on-board EEPROM. As revisions evolved, some of the fields became dynamic (such as temperature or optical power readings), while others (such as interrupts and alarms) became Read/Write (R/W). As a result, an EEPROM based implementation does not suffice anymore, although the term is still used to refer to the Memory Map.

Consequently, the Samtec current implementation, although referred to as an “EEPROM map”, does not use an actual direct EEPROM read or write. Instead, each I2C read or write request is interpreted by the embedded microprocessor in the optical engine. The microprocessor then reads or stores data which could come from, or go to different sources:

- The processor’s own internal EEPROM
- The processor’s static, dynamic RAM or register memory
- Sensors or internal chipset readings
- Internal processor calculations or registers

An important consequence is that EEPROM byte addresses used in two wire interface requests are virtual – they will not always correspond to the physical address in the processor internal EEPROM, or might not have a physical EEPROM location at all. This is invisible to the end user, who just reads and writes to the I^2C as if it were an actual EEPROM according to the standard Memory Map. The processor will take care of fetching and writing the data internally from/to the correct physical location.

The structure of the memory map is shown in Figure 35. Each address contains one lower page and four upper pages per address. Each page contains 128 bytes of address space. Page 00 (lower and upper) contain the most accessed functionality.

This structure permits timely access to fields in the lower page, which contain time-critical information, such interrupt flags, alarms, critical monitors and per-lane control. Read-only device information such as serial ID information and vendor information is available in Upper Page 00, which is similar for both transmit and receive devices.

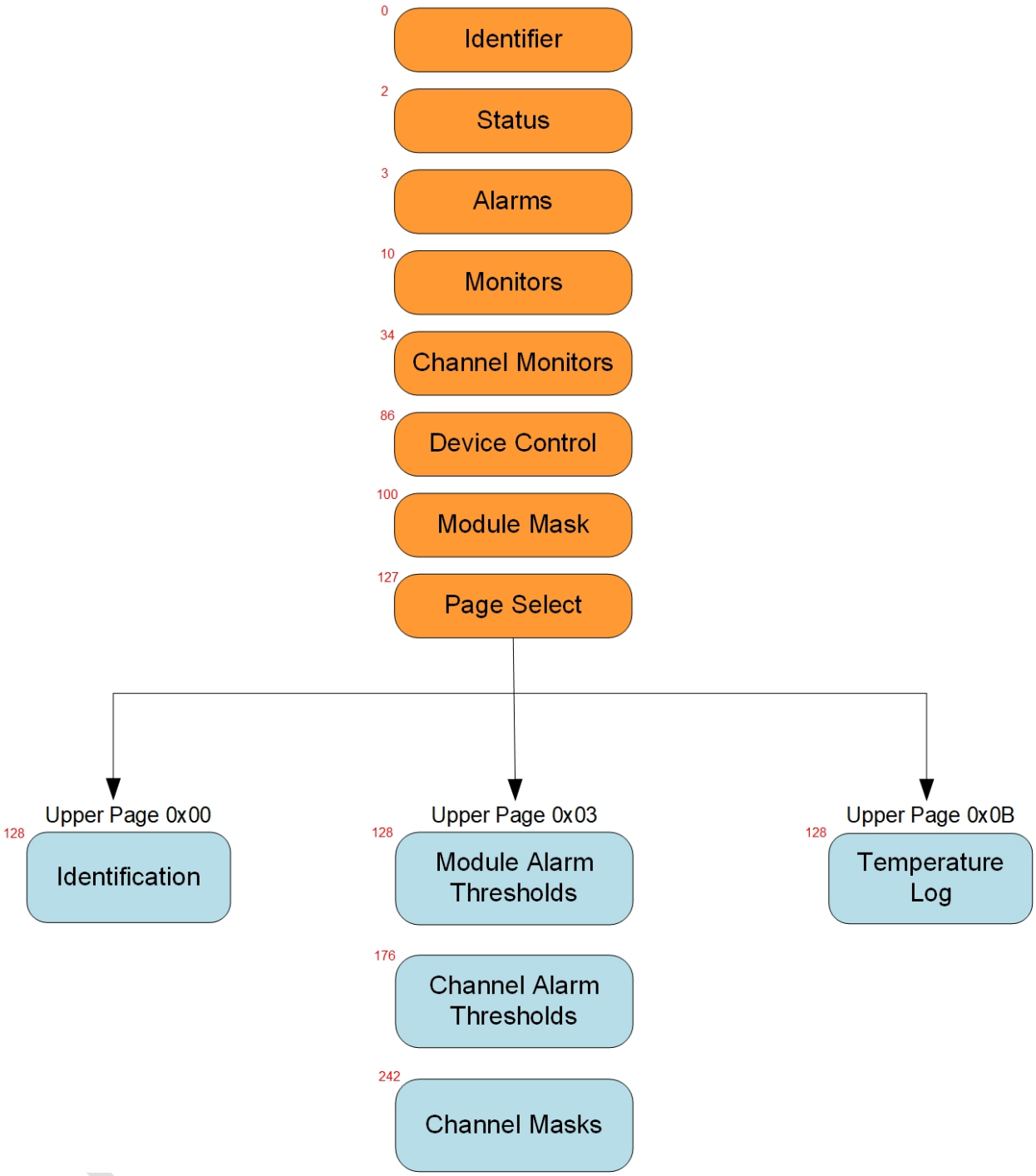


Figure 34: FireFly 28G x4 Optical Assembly Memory Map

13.2.1 Module Memory Map

The lower 128 bytes of the 2-wire serial bus address space is used to access a variety of measurement and diagnostic functions, a set of control functions, and a means to select which of the various upper memory map pages are accessed on subsequent reads. This portion of the address space is always directly addressable and is used for monitors and control functions that may need to be repeatedly accessed.

Address	Type	Name	Description	Default Value
0	RO	Identifier		0x81
1	-	Reserved		-
2	RO	Status	See Table 26	0x00
3	RO	Loss of Signal Alarms	See Table 27	0x00
4	RO	Transmit Fault Alarms	See Table 28	0x00
5	RO	CDR Loss of Lock Alarms	See Table 29	-
6	RO	Temperature Alarms	See Table 30	0x00
7	RO	$VCC_{3.3}$ and $VCC_{1.8}$ Alarms	See Table 31	0x00
8	-	Reserved		-
9-10	RO	Received Power Alarms	See Table 32	0x00
11-18	-	Reserved		-
19-20	RO	Elapsed Operating Time	16-bit unsigned integer [2 hours]	-
21	-	Reserved		-
22	RO	Internal Temperature	Signed bit twos complement	-
23-25	-	Reserved		-
26-27	RO	$Vcc_{3.3}$	16-bit unsigned integer [100 µV]	-
28-29	RO	$Vcc_{1.8}$	16-bit unsigned integer [100 µV]	-
30-33	-	Reserved		-
34-35	RO	Rx1 Measured Optical Power	16-bit unsigned integer [0.1 µW] Accuracy ± 3 dB (RSSI)	-
36-37	RO	Rx2 Measured Optical Power		-
38-39	RO	Rx3 Measured Optical Power		-
40-41	RO	Rx4 Measured Optical Power		-
42-68	-	Reserved		-
69-71	RO	Firmware Revision		
70	RO	Firmware Version, Minor		
71	RO	Firmware Revision		
72-85	-	Reserved		-
86	R/W	Transmit Channel Disable	See Table 33	0x00
87-97	-	Reserved		-
98	R/W	CDR Enable	See Table 34	0xFF
99	RO	Reserved		-
100	R/W	Mask LOS alarms	See Table 36	0x00
101	R/W	Mask Tx Fault Alarms	See Table 37	0x00
102	R/W	Mask CDR LOL alarms	See Table 38	0x00
103	R/W	Mask Temp Alarms/ Warnings	See Table 39	0x00
104	R/W	Mask $VCC_{3.3}$ and $VCC_{1.8}$ Alarms / Warnings	See Table 40	0x00
105-126	-	Reserved		-
127	R/W	Page Select Byte		0x00

Table 25: Lower Page 0x00

Status Bytes

Bytes 3 through 18 are status bytes where the status of LOS, Tx Fault, $VCC_{3.3}$ and $VCC_{1.8}$ alarms, internal temperature and received optical power alarms are reported. For normal operation and default state, the bits in this field have the value of 0b. When an alarm occurs, the field corresponding to this alarm is changed to 1b. Once asserted, the bits remained set (latched) until cleared by a read operation that includes the affected bit or reset by the ResetL pin.

Fault bits that are cleared while the underlying fault persists MAY be immediately set again by the module. This may or may not cause the IntL to de-assert and then re-assert quickly.

Bit	Name	Description	Default
7-6		Reserved	0
5		Reserved	0
4		Reserved	0
3		Reserved	0
2		Reserved	0
1	INTL Status	1 = IntL output pin is asserted 0= IntL output pin is de-asserted	0
0	Data_Not_Ready	1 = engine has not yet achieved power up and memory is not ready 0 = data is ready to be read	0

Table 26: Status Information Byte 2

Interrupt Bytes

Bytes 3-21 consist of interrupt flags for LOS, TX Fault, warnings and alarms. The non-asserted state is 0b. If an interrupt flag condition is true, the corresponding flag bit will be set to 1b. The flag bit will remain set until the host performs a read operation of the bit or the optical engine is reset.

Flag bits cleared while the underlying interrupt condition remains true may be immediately set again by the free side device. During this process the IntL pin may be re-asserted if the associated mask bit is not set. These flags may be masked.

Bit	Name	Description	Default
7	Tx4 LOS	Latched Loss of Signal alarm 0 = Normal operation 1 = Loss of Signal	0
6	Tx3 LOS		0
5	Tx2 LOS		0
4	Tx1 LOS		0
3	Rx4 LOS		0
2	Rx3 LOS		0
1	Rx2 LOS		0
0	Rx1 LOS		0

Table 27: Loss of Signal Alarm Byte 3

Bit	Name	Description	Default
7-4	Reserved		-
3	Tx4 Fault	Latched transmitter fault alarm 0 = Normal Operation 1 = Loss of Signal	0
2	Tx3 Fault		0
1	Tx2 Fault		0
0	Tx1 Fault		0

Table 28: Tx Fault Byte 4

Bit	Name	Description	Default
7	Tx4 LOL	Latched Loss of CDR Lock alarm 0 = Normal Operation 1 = Loss of CDR lock	0
6	Tx3 LOL		0
5	Tx2 LOL		0
4	Tx1 LOL		0
3	Rx4 LOL		0
2	Rx3 LOL		0
1	Rx2 LOL		0
0	Rx1 LOL		0

Table 29: Byte Loss of Lock Alarm Byte 5

Bit	Name	Description	Default
7	Temperature High Alarm	Temperature High/Low Alarms/Warnings 0 = Normal Operation 1 = Temperature Alarm/Warning	0
6	Temperature Low Alarm		0
5	Temperature High Warning		0
4	Temperature Low Warning		0
3-1	Reserved		-
0	Int Complete Flag	Value of 1 when module has experience a reset or at power up	0

Table 30: Temperature Alarms and Warnings Byte 6

Bit	Name	Description	Default
7	$Vcc_{3.3}$ High Alarm	Voltage High/Low Alarms/Warnings 0 = Normal Operation 1 = Voltage Alarm/Warning	0b
6	$Vcc_{3.3}$ Low Alarm		0b
5	$Vcc_{3.3}$ High Warning		0b
4	$Vcc_{3.3}$ Low Warning		0b
3	$Vcc_{1.8}$ High Alarm		0b
2	$Vcc_{1.8}$ Low Alarm		0b
1	$Vcc_{1.8}$ High Warning		0b
0	$Vcc_{1.8}$ Low Warning		0b

Table 31: $VCC_{3.3}$ and $VCC_{1.8}$ Alarms and Warnings Byte 7

Byte	Bit	Name	Description	Default
9	7	Rx1 Power High Alarms	Received power alarm 0 = Normal Operation 1 = Power Alarm/Warning	0
	6	Rx1 Power Low Alarm		0
	5	Rx1 Power High Warning		0
	4	Rx1 Power Low Warning		0
	3	Rx2 Power High Alarms		0
	2	Rx2 Power Low Alarm		0
	1	Rx2 Power High Warning		0
	0	Rx2 Power Low Warning		0
10	7	Rx3 Power High Alarms		0
	6	Rx3 Power Low Alarm		0
	5	Rx3 Power High Warning		0
	4	Rx3 Power Low Warning		0
	3	Rx4 Power High Alarms		0
	2	Rx4 Power Low Alarm		0
	1	Rx4 Power High Warning		0
	0	Rx4 Power Low Warning		0

Table 32: Low Power Alarms and Warning Bytes 9-10

Monitors

Real time monitoring for the FireFly x4 optical assembly includes case temperature, supply voltage, and elapsed operating time.

Elapsed Operating Time [bytes 19 and 20] is represented as a 16-bit unsigned integer with the time defined as the full 16 bit value (0 – 65535) with LSB equal to 2 hours, yielding a total measurement range of 0 to 131,070 hours or >14 years. Accuracy is ± 10%.

Internally measured temperature [byte 22] is represented as an 8-bit signed two's complement value in increments of 1 °C, yielding a total range of –127 °C to +127 °C that is considered valid between -40 °C and 85 °C. Accuracy is ± 5 °C

Internally measured module supply voltage [bytes 26 and 27] is represented as a 16-bit unsigned integer with the voltage defined as the full 16-bit value (0 – 65535) with LSB equal to 100 µVolt, yielding a total measurement range of 0 to 6.55 Volts. Accuracy is ± 0.1 V.

Received Optical Power per channel [bytes 34-41] is represented in mW as the average received power. The received power value is encoded as a 16-bit unsigned integer with the power defined as the full 16-bit value (0 to 65535) with LSB equal to 0.1 µW, yielding a total measurement range of 0 to 6.5535mw (~0 to 8.2 dBm). Accuracy is ± 3 dB over the temperature and voltage.

Control

Bit	Name	Description	Default
7-4	Reserved		-
3	Channel Disable Tx-04	Writing 1 will disable channel.	0b
2	Channel Disable Tx-03	Channel will stay disabled until enabled by writing 0, or via reset	0b
1	Channel Disable Tx-02		0b
0	Channel Disable Tx-01		0b

Table 33: Transmit Channel Disable Byte 86

Bit	Name	Description	Default
7	Tx4 CDR Enable	1= CDR enabled	1b
6	Tx3 CDR Enable	0 = CDR Bypassed	1b
5	Tx2 CDR Enable		1b
4	Tx1 CDR Enable		1b
3	Rx4 CDR Enable		1b
2	Rx3 CDR Enable		1b
1	Rx2 CDR Enable		1b
0	Rx1 CDR Enable		1b

Table 34: CDR Enable Byte 98

Mask Bytes

The host system may control which flags trigger an interrupt (IntL) by setting individual bits from a set of masking bits in bytes 100 -106 of the lower page 0x00. A "1" value in a masking bit prevents the assertion of the hardware IntL pin by the corresponding latched flag bit. Masking bits are volatile and start up with all unmasked ("0"). Additional latching capability is available on the upper page 0x03.
The mask bits may be used to prevent continued interruption from on-going conditions, which would otherwise continually re-assert the hardware IntL pin. A mask bit is provided whenever the associated flag bit is implemented.

Bit	Name	Description	Default
7	Mask Tx4 LOS alarm	Writing 1 prevents INTL on LOS alarm. Default =0.	0b
6	Mask Tx3 LOS alarm		0b
5	Mask Tx2 LOS alarm		0b
4	Mask Tx1 LOS alarm		0b
3	Mask Rx4 LOS alarm		0b
2	Mask Rx3 LOS alarm		0b
1	Mask Rx2 LOS alarm		0b
0	Mask Rx1 LOS alarm		0b

Table 35: LOS Alarm Mask Byte 100

Bit	Name	Description	Default
7-4	Reserved		-
3	Mask Tx4 Fault alarm	Writing 1 prevents INTL on Tx Fault Alarm. Default =0	0b
2	Mask Tx3 Fault alarm		0b
1	Mask Tx2 Fault alarm		0b
0	Mask Tx1 Fault alarm		0b

Table 36: Tx Fault Alarm Mask Byte 101

Bit	Name	Description	Default
7	Mask Tx4 CDR LOL alarm	Writing 1 prevents INTL on CDR LOL alarm. Default =0.	0b
6	Mask Tx3 CDR LOL alarm		0b
5	Mask Tx2 CDR LOL alarm		0b
4	Mask Tx1 CDR LOL alarm		0b
3	Mask Rx4 CDR LOL alarm		0b
2	Mask Rx3 CDR LOL alarm		0b
1	Mask Rx2 CDR LOL alarm		0b
0	Mask Rx1 CDR LOL alarm		0b

Table 37: CDR LOL Alarm Mask Byte 102

Bit	Name	Description	Default
7	Mask Temp High alarm	Writing 1 prevents INTL on Temp High / Low alarm and warning. Default =0.	0b
6	Mask Temp Low alarm		0b
5	Mask Temp High warning		0b
4	Mask Temp Low warning		0b
3-0	Reserved		-

Table 38: Temperature Alarms and Warning Mask Byte 103

Bit	Name	Description	Default
7	Mask $Vcc_{3.3}$ High alarm	Writing 1 prevents INTL on $VCC_{3.3}$ High / Low alarm and warning. Default =0.	0b
6	Mask $Vcc_{3.3}$ Low alarm		0b
5	Mask $Vcc_{3.3}$ High warning		0b
4	Mask $Low_{3.3}$ Low warning		0b
3	Mask $Vcc_{1.8}$ High alarm	Writing 1 prevents INTL on $VCC_{1.8}$ High / Low alarm and warning. Default =0.	0b
2	Mask $Vcc_{1.8}$ Low alarm		0b
1	Mask $Vcc_{1.8}$ High warning		0b
0	Mask $Low_{1.8}$ Low warning		0b

Table 39: $VCC_{3.3}$ and $VCC_{1.8}$ Alarms and Warning Mask Byte 104

13.2.2 Upper Page 0x00

The Upper page 0x00 consists of read only information that describes the cable performance capabilities, technology and length as well as vendor information. **Table 40** describes in detail all the bytes of the upper page 0x00 together with their default value when applicable.

Address	Type	Name	Description	Default
128-167	-	Reserved	-	-
168-180	RO	Part Number	13-character ASCII field, left aligned and padded on the right with an ASCII space	-
184-189	-	Reserved	-	-
190	RO	Max case temperature	85 °C	0x00
191-195	-	Reserved	-	-
196-205	RO	Vendor serial number	10 Characters ASCII field, left aligned and padded on the right with ASCII spaces (0x20)	-
206-223	-	Reserved	-	-
224-255	-	Reserved	-	-

Table 40: Upper Page 0x00 Overview

13.2.3 Upper Page 0x02

Samtec provides the ability to change the default address for the two-wire interface. Byte 255 of upper page two is used for this and is non-volatile.

Address	Type	Name	Function
128-254		Reserved	
255	R/W	See Section 13.1	TWI Address

Table 41: Upper Page 02 Overview

13.2.4 Upper Page 0x03

Upper Page 0x03 provides Module Alarm Thresholds plus capacity for future Channel Alarm Threshold functionality. High and Low threshold values for the module alarms are stored in read-only memory in bytes 128 – 175 of the Upper Page 0x03 as shown in Table 42. This factory pre-set values correspond to the values at which the module alarms (Bytes 22-39) are triggered as performance is not guaranteed. If no corresponding mask is set, then the IntL signal will be triggered.

Address	Type	Name	Description	Default
128	RO	Temp Alarm Threshold Hi	8-bit signed two's complement integer [100 °C]	0x64
129	-	Reserved		-
130	RO	Temp Alarm Threshold Low	8-bit signed two's complement integer [-40 °C]	0xD8
131	-	Reserved		-
132	RO	Temp Alarm Warning Hi	8-bit signed two's complement integer [100 °C]	0x64
133	-	Reserved		-
134	RO	Temp Alarm Warning Low	8-bit signed two's complement integer [-40 °C]	0xD8
135-143	-	Reserved		-
144-145	RO	$VCC_{3.3}$ Alarm Threshold Hi	16-bit unsigned integer in 100 µV units Value = 3.465 V	0x875A
146-147	RO	$VCC_{3.3}$ Alarm Threshold Lo	16-bit unsigned integer in 100 µV units Value = 3.135 V	0x7A76
148-149	RO	$VCC_{3.3}$ Warning Threshold Hi	16-bit unsigned integer in 100 µV units Value = 3.465 V	0x875A
150-151	RO	$VCC_{3.3}$ Warning Threshold Lo	16-bit unsigned integer in 100 µV units Value = 3.135 V	0x7A76
152-153	RO	$VCC_{1.8}$ Alarm Threshold Lo	16-bit unsigned integer in 100 µV units Value = 1.71 V	0x49D4
154-155	RO	$VCC_{1.8}$ Warning Threshold Hi	16-bit unsigned integer in 100 µV units Value = 1.89 V	0x42CC
156-157	RO	$VCC_{1.8}$ Warning Threshold Lo	16-bit unsigned integer in 100 µV units Value = 1.71 V	0x49D4
158-159	RO	$VCC_{1.8}$ Alarm Threshold Hi	16-bit unsigned integer in 100 µV units Value = 1.89 V	0x42CC
160-175	-	Reserved		-
176-177	RO	Rx Power Alarm Threshold Hi	16-bit unsigned integer in 0.1 µW units Value = 2.188 mW (3.4 dBm)	0x5578
178-179	RO	Rx Power Alarm Threshold Low	16-bit unsigned integer in 0.1 µW units Value = 0.089 mW (-10.5 dBm)	0x037A
180-181	RO	Rx Power Warning Threshold Hi	16-bit unsigned integer in 0.1 µW units Value = 2.188 mW (3.4 dBm)	0x5578
182-183	RO	Rx Power Warning Threshold Low	16-bit unsigned integer in 0.1 µW units Value = 0.089 mW (-10.5 dBm)	0x037A
184-225	-	Reserved		-
226	R/W	Channel Polarity	See Table 44	0x00
227-233	-	Reserved		-
234-235	R/W	Transmit Input Equalisation	See Table 45	0x00
236-237	R/W	Receive Output Pre-emphasis	See Table 46	0x00
238-239	R/W	Rx Output Amplitude	See Table 47	0x00
240	R/W	Squelch Disable	See Table 48	0x00
241	R/W	Receiver Output Disable	See Table 49	0x00
242-243	R/W	Mask Rx Power High Alarm	See Table 50	0x00
244-255	-	Reserved		-

Table 42: Upper Page 0x03 Overview

Channel Controls

Bit	Name	Description	Default
7	Polarity Rx4	Individual channel polarity control 0 = Channel not inverted 1 = Channel Inverted	0b
6	Polarity Rx3		0b
5	Polarity Rx2		0b
4	Polarity Rx1		0b
3	Polarity Tx4		0b
2	Polarity Tx3		0b
1	Polarity Tx2		0b
0	Polarity Tx1		0b

Table 43: Channel Polarity Control Byte 226

Byte	Bit	Name	Description	Default
234	7-4	Tx1 Input Equalisation	Transmitter Input equalization levels 1111-1011: Reserved 1010 = 9.8 dB 1001 = 8.8 dB 1000 = 8.2 dB 0111 = 7.2 dB 0110 = 6.5 dB 0101 = 4.8 dB 0100 = 3.7 dB 0011 = 2.7 dB 0010 = 1.9 dB 0001 = 1.3 dB 0000 = 1.3 dB (default)	0000b
	3-0	Tx2 Input Equalisation		
235	7-4	Tx3 Input Equalisation		
	3-0	Tx4 Input Equalisation		

Table 44: Transmit Input Equalisation Control Bytes 234-235

Byte	Bit	Name	Description	Default
236	7-4	Rx1 Output de-emphasis	Receiver Output Equalisation levels 1111-1000: Reserved 0111 = 7.5 dB 0110 = 6 dB 0101 = 5 dB 0100 = 4 dB 0011 = 3 dB 0010 = 2 dB 0001 = 1 dB 0000 = No Equalisation (default)	0000b
	3-0	Rx2 Output de-emphasis		
237	7-4	Rx3 Output de-emphasis		
	3-0	Rx4 Output de-emphasis		

Table 45: Receiver Output Pre-Emphasis Control Bytes 236-237

Byte	Bit	Name	Description	Default
238	7-4	Rx1 Output Amplitude	Global parameter for the four output channel amplitudes. 0000 = 300 mV (default) 0001 = 450 mV 0010 = 600 mV 0011 = 900 mV 0100 – 1111 = reserved	0000b
	3-0	Rx2 Output Amplitude		
239	7-4	Rx3 Output Amplitude		
	3-0	Rx4 Output Amplitude		

Table 46: Receive Output Amplitude Bytes 238-239

Bit	Name	Description	Default
7	Rx4 Squelch Disable	Individual channel squelch control 0 = Squelch enable 1 = Squelch disable	0b
6	Rx3 Squelch Disable		0b
5	Rx2 Squelch Disable		0b
4	Rx1 Squelch Disable		0b
3	Tx4 Squelch Disable		0b
2	Tx3 Squelch Disable		0b
1	Tx2 Squelch Disable		0b
0	Tx1 Squelch Disable		0b

Table 47: Transmit and Receive Squelch Control Byte 240

Bit	Name	Description	Default
7	Rx4 Output Enable	Receiver Output Enable 0 = Output Enable 1 = Output Disable	0b
6	Rx3 Output Enable		0b
5	Rx2 Output Enable		0b
4	Rx1 Output Enable		0b
3-0	Reserved		-

Table 48: Receiver Output Disable Byte 241

Channel Monitor Masks

Byte	Bit	Name	Description	Default
242	7	Mask Rx1 Power High Alarm	Writing “1” prevents Rx power alarm	0
	6	Mask Rx1 Power Low Alarm		0
	5	Mask Rx1 Power High Warning		0
	4	Mask Rx1 Power Low Warning		0
	3	Mask Rx2 Power High Alarm		0
	2	Mask Rx2 Power Low Alarm		0
	1	Mask Rx2 Power High Warning		0
	0	Mask Rx2 Power Low Warning		0
243	7	Mask Rx3 Power High Alarm		0
	6	Mask Rx3 Power Low Alarm		0
	5	Mask Rx3 Power High Warning		0
	4	Mask Rx3 Power Low Warning		0
	3	Mask Rx4 Power High Alarm		0
	2	Mask Rx4 Power Low Alarm		0
	1	Mask Rx4 Power High Warning		0
	0	Mask Rx4 Power Low Warning		0

Table 49: Receiver Power Alarm and Warning Mask Bytes 242 - 243

13.2.5 Upper Page 0x0B

Time at temperature information is provided for possible end of life prediction. Time at temperature bytes are represented as a 24-bit unsigned integer with the time defined as the full 24-bit value (0 – 65535) with LSB (higher byte) equal to 5 minutes. These time at temperature bytes are updated every two hours to ensure that the total time at temperature recorded is equal to the Elapsed Operating Time recorded in bytes 38-39.

A peak temperature monitor is also provided. This temperature is recorded as an 8-bit unsigned integer corresponding to the maximum recorded case temperature [°C]. Accuracy is ± 3°C.

Address	Type	Name	Function
128-130	RO	Time at Temperature < 0°C	Temperature Monitors
131-133	RO	0 °C ≤ Time at Temperature < 5 °C	
134-136	RO	5 °C ≤ Time at Temperature < 10 °C	
137-139	RO	10 °C ≤ Time at Temperature < 15 °C	
140-142	RO	15 °C ≤ Time at Temperature < 20 °C	
143-145	RO	20 °C ≤ Time at Temperature < 25 °C	
146-148	RO	25 °C ≤ Time at Temperature < 30 °C	
149-151	RO	30 °C ≤ Time at Temperature < 35 °C	
152-154	RO	35 °C ≤ Time at Temperature < 40 °C	
155-157	RO	40 °C ≤ Time at Temperature < 45 °C	
158-160	RO	45 °C ≤ Time at Temperature < 50 °C	
161-163	RO	50 °C ≤ Time at Temperature < 55 °C	
164-166	RO	55 °C ≤ Time at Temperature < 60 °C	
167-169	RO	60 °C ≤ Time at Temperature < 65 °C	
170-172	RO	65 °C ≤ Time at Temperature < 70 °C	
173-175	RO	70 °C ≤ Time at Temperature < 75 °C	
176-178	RO	75 °C ≤ Time at Temperature < 80 °C	
179-181	RO	80 °C ≤ Time at Temperature < 85 °C	
182-184	RO	85 °C ≤ Time at Temperature < 90 °C	
185-187	RO	90 °C ≤ Time at Temperature < 95 °C	
188-190	RO	95 °C ≤ Time at Temperature < 100 °C	
191-193	RO	Time at Temperature > 100 °C	
194	RO	Peak Temperature Monitor	
195-255	-	Reserved	Reserved

Table 50: Upper Page 0Bh Overview

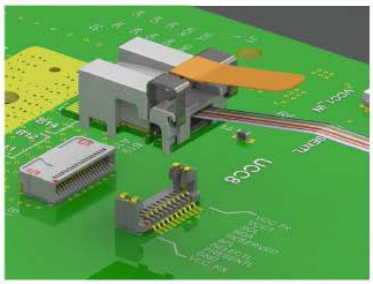
14 Appendix I: Insertion and Removal

FIREFLY™
Micro Flyover System

Insertion Instructions

1

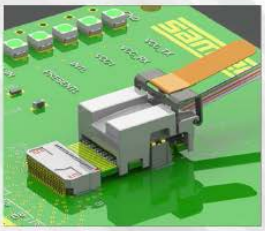
Align optical or copper assembly so notches in PCB are over the positive latching receptacle.



Unmated (Latch Open)

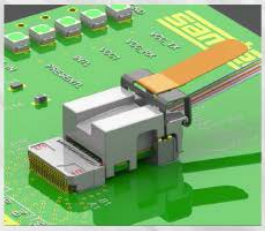
2

Drop the cable assembly down keeping it parallel to the board.

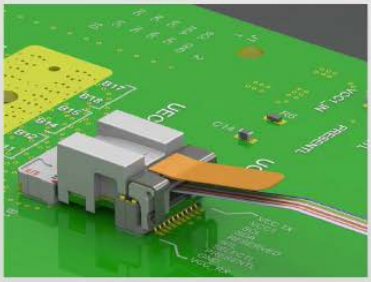


3

Slide the cable assembly forward keeping it level to the board.

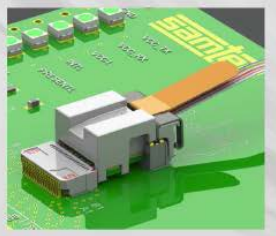


Mated (Latch Down)



4

Continue sliding the cable assembly until fully engaged.



FIREFLY™

INSERTION AND REMOVAL INSTRUCTIONS

Requires Firefly™ Insertion Tool
CAT-IN-ECUO-02
(Instruction Sheet STS-N-009)

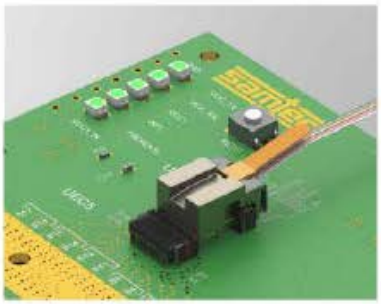
1. Align tooling with cable assembly so that notches in PCB are over the positive latching receptacle.

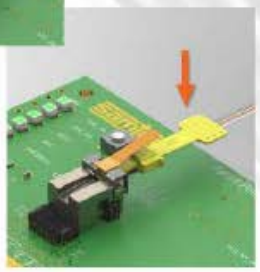
2. Drop tooling with cable assembly down keeping it parallel to board.

3. Slide tooling with cable assembly forward keeping it level to board until fully engaged.

4. To remove tool press the side button and lean tool slightly to the right and lift tool upwards.

Mated (Latch Down)





5. Remove by pulling the latch position retainer.

15 Appendix II: Connector Cleaning

OPTICS CLEANING INSTRUCTIONS

CLEANING STICK: REFERENCE PART NUMBER USCONEC 7104

STEP 1

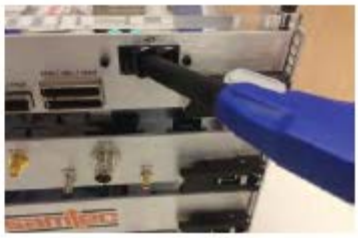
- To clean connector, remove cover and insert connector into cap.

STEP 2

- Press connector toward the cleaner until an audible click is heard, indicating a successful cleaning process.

STEP 3

- To clean panel mounted housing, remove cap and insert tip into housing. Press the cleaning tool into the connector until an audible click is heard, indicating a successful cleaning process.



CASSETTE CLEANER: REFERENCE PART NUMBER USCONEC 6226

STEP 1

- Refillable Cassette Cleaner.

STEP 2

- Depress green lever to expose cleaning cloth. Run the end of the connector along the cloth in the direction of the arrow.

STEP 3

- Reactivate green lever, rotate connector 180° degrees and run the end of the connector along the cloth in the direction of the arrow again.

OPTICS CLEANING INSTRUCTIONS
DISPOSABLE CLEANERS

GEL STICK CLEANER: REFERENCE PART NUMBER SENKO SCK-PT-MPO-GSC

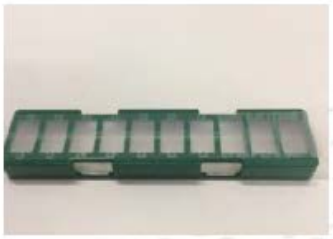
STEP 1
- Gel Stick Cleaner

STEP 2
- Remove cap and line up stick with bulkhead connector.

STEP 3
- Press stick firmly into bulkhead connector (do not use stick cleaner more than once).

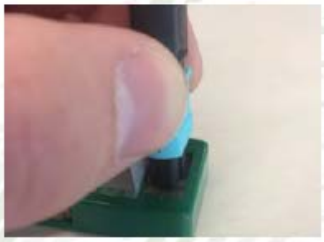
GEL PAD CLEANER: REFERENCE PART NUMBER SCK-PT-MPO-01

STEP 1
- Gel Pad Cleaner



STEP 2
- Peel back tape exposing one pad (do not expose more pads than you plan to use).

STEP 3
- Press MPO connector firmly into gel pad (do not use one gel pad more than twice per connector).



Several online resources are available with further information on the inspection and cleaning of optical connectors available on the web. See http://www.panduit.com/heiler/InstallInstructions/N-FBFS061--Rev0--ENG.pdf for an example.

Box 1147 • New Albany, IN 47151-1147 USA
+1-800-SAMTEC-9 (USA & Canada) • Tel: +1-812-944-6733 • Fax: +1-812-948-5047 • Email: info@samtec.com

SAMTEC NORTHERN CALIFORNIA
2323 Owen St, • Suite 120 • Santa Clara, CA 95054
Tel: +1-800-SAMTEC-9 • Fax: +1-408-217-5172 • Email: samtecsiliconvalley@samtec.com

SAMTEC SOUTHERN CALIFORNIA
5410 Trabuco Road • Suite 120 • Irvine, CA 92620
Tel: +1-800-726-8329 • Email: samtecsoutherncalifornia@samtec.com

SAMTEC SOUTH AMERICA
Rua Alagoas Nr 1460 • Sala 805 • Bairro Savassi • Belo Horizonte - Minas Gerais 30130-160 • Brazil
Tel: +55 31 3786 3227 • Fax: +55 31 3786 3229 • Email: brazilsales@samtec.com

SAMTEC UNITED KINGDOM
11 Mollins Court• Westfield, Cumbernauld • Scotland G68 9HP
Tel: +44 01236 739292 • Fax: +44 01236 727113 • Email: scotland@samtec.com

SAMTEC GERMANY
Streiflacher Str. 7 • 82110 Germering • Germany • +0800 SAMTEC9 (+0800 / 72 68 329) Germany only
Tel: +49 (0) 89 / 89460-0 • Fax: +49 (0) 89 / 89460-299 • Email: germany@samtec.com

SAMTEC FRANCE
Val d' Europe Park • 11, rue du Courtalin - Bâtiment B • 77700 Magny le Hongre • France
Tel: +33 1 60 95 06 60 • Fax: +33 1 60 95 06 61 • Email: france@samtec.com

SAMTEC ITALY
Via Colleoni 25 • Centro Direzionale Colleoni • Palazzo Pegaso Ingresso 3 • 20864 Agrate Brianza-Monza Brianza (MB) • Italy
Tel: +39 039 6890337 • Fax: +39 039 6890315 • Email: italy@samtec.com

SAMTEC NORDIC/BALTIC
Solkraftsvägen 25 • 13570 Stockholm • Sweden
Tel: +46 8 4477280 • Fax: +46 8 7420413 • Email: scandinavia@samtec.com

SAMTEC BENELUX
11 Mollins Court• Westfield, Cumbernauld • Scotland G68 9HP
Tel: +44 01236 739292 • Fax: +44 01236 727113 • Email: benelux@samtec.com

SAMTEC ISRAEL
21 Bar-Kochva St. • Concord Tower • B'nei Brak, Israel 51260
Tel: +972 3 7526600 • Fax: +972 3 7526690 • Email: israel@samtec.com

SAMTEC INDIA
#11, 2nd Floor, Chetana, Dattatreya Road • Basavanagudi • Bangalore • 560 004 India
Tel: +91 80 3272 1612 • Fax: +91 80 2662 0967 • Email: india@samtec.com

SAMTEC ANZ
2A San Antonio Court • Mentone 3194 • Victoria, Australia
Tel: +613 9580 0683 • Fax: +613 9580 0684 • Email: australia@samtec.com

SAMTEC SINGAPORE
1 Kallang Sector #05-01/02 • Kolam Ayer Industrial Park • Singapore 349276
Tel: +65 6745 5955 • Fax: +65 6841 1502 • Email: singapore@samtec.com

SAMTEC JAPAN
Nisso No. 16 Bldg. • 3-8-8, Shinyokohama, Kohoku-ku • Yokohama-shi, Kanagawa 222-0033 Japan
Tel: +81 45 475 1385 • Fax: +81 45 475 1340 • Email: japan@samtec.com

SAMTEC SHANGHAI
Unit 601, Qilai Building • No 889 Yishan Road • Shanghai, China 200233
Tel: +86 21 6083 3766 • Fax: +86 21 5423 4575 • Email: china@samtec.com

SAMTEC SHENZHEN
Rm 906B 9/F New World Center Tower • Yi Tian Road, Fu Tian District • Shenzhen, China 518026
Tel: +86 755 83776780 • Fax: +86 755 83776767 • Email: hongkong@samtec.com

SAMTEC TAIWAN
10F, No. 182, Sec. 2 • Dunhua S. Rd. • Da-an District • Taipei City 10669 • Taiwan (R.O.C.)
Tel: 00801 14 9916 (Taiwan only) • Tel: +886 2 2735 6109 • Fax: +886 2 2735 5036 • Email: taiwan@samtec.com

SAMTEC HONG KONG
Room 18, 13/F, Shatin Galleria • 18-24 Shan Mei Street • Fo Tan, Shatin, Hong Kong
Tel: +852 26904858 • Fax: +852 26904842 • Email: hongkong@samtec.com

SAMTEC KOREA
RM#758, Sungwoo Starwoos Officetel Gumi-dong • Seongnam Si, Bundang-gu, Gyeonggi-Do • 463-860 South Korea
Tel: +82 31 717 5685 • Fax: +82 31 717 5681 • Email: korea@samtec.com

SAMTEC ONLINE
www.samtec.com

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